MILLIMETER-WAVE AND TERAHERTZ SIGNAL GENERATION AND DETECTION IN SILICON

A Dissertation
Presented to
The Academic Faculty

by

Taiyun Chi

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
December 2017

MILLIMETER-WAVE AND TERAHERTZ SIGNAL GENERATION AND DETECTION IN SILICON

Approved by:

Dr. Hua Wang, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Muhannad S. Bakir
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Andrew F. Peterson
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. John Papapolymerou
Department of Electrical and Computer Engineering
Michigan State University

Dr. Ali Adibi
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Piet Wambacq
IMEC

Date Approved: October 27, 2017

To My Family

ACKNOWLEDGEMENTS

It is hard for me to believe that my Ph.D. study at Georgia Tech has come to an end. When I look back, my time at Georgia Tech could never be so enjoyable and fulfilling without the generous support from many great people. I wish to express my sincere gratitude to them here.

I am extremely fortunate and indebted to have Prof. Hua Wang as my Ph.D. advisor. Hua has been a great advisor, mentor, teacher and friend. I really enjoy his research philosophy that always strives for true innovations and long-term impact to the society. At the initial stage of my Ph.D. study, Hua provided substantial technical advice to help me get a quick start. He even landed the probe for me when I measured my first 500GHz signal generation chip! After that, I have been given full freedom to pursue many different research areas and I sincerely appreciate his trust and support over the years. Moreover, Hua has provided me with many opportunities to participate in proposal writings and lead the research projects in our group. These experiences have been extremely beneficial to broaden my research horizons, think in a bigger picture, and build my leadership. Beyond academics, Hua's wisdom, enthusiasm, and ambition have been and will continue inspiring me for excellence throughout my career. I hope that I have learned some of these from him.

I would also like to thank my other thesis committee members: Dr. John Papapolymerou, Dr. Muhannad Bakir, Dr. Andrew Peterson, Dr. Ali Adibi, and Dr. Piet Wambacq. I have been involved in several collaborative projects with Prof. Papapolymerou and Prof. Bakir on high-frequency signal generation and integrated bio-electronics interface, and I want to thank them for their guidance, comments and feedbacks. Prof.

Peterson's Applied Electromagnetics class has been extremely helpful and laid a solid background for my Ph.D. research in mm-wave/THz IC design. Taking Prof. Adibi's Integrated Optics class was a great experience in summer 2014. His teaching is not only very intuitive, but also rigorous in mathematics, which I consider as one of the best courses I have ever taken. I got to know Dr. Wambacq during the ISSCC conference. As an internationally renowned researcher in the field of IC design, the encouragement and support from Piet are greatly appreciated.

Georgia Tech is a wonderful place for interdisciplinary research. I was very fortunate to have the opportunities to work with Prof. Todd McDevitt and Prof. Mark Styczynski in my multi-modality biosensor project. I am also indebted to their students, Jessica Butts, Dr. Tracy Hookway, and Amy Su. Without their expertise in biomedical engineering and critical contributions, the project can never be so successful.

Part of my Ph.D. research is to develop a sub-millimeter-scale low-power radio for Internet-of-Things (IoT) devices and "invisible" field-deployable sensor networks using THz frequency. This is a collaborative project with Prof. Foster Dai's group at Auburn University. I want to thank Foster and his student Hechen Wang for their active involvement and great efforts.

As one of the first batch of Ph.D. students in the Georgia Tech Electronics and Micro-System (GEMS) Lab, I have witnessed the growth of our group. When I first joined the group in 2012, there was literally nothing in the lab except several pieces of unopened Agilent equipment. As of today, we have grown to a large research group with 14 Ph.D.

students, and well-equipped with world-class testing facilities. I am very proud to see the tremendous achievements of our group over the years.

It has been a privilege working with talented colleagues in our group. I want to thank Dr. Song Hu for his assistance at my early stage of Ph.D. study. I am very fortunate to have Jong Seok Park as my colleague and moreover a great friend. We have been working together for many many research projects, and I have benefitted a lot from his strong work ethic and helpful technical discussions. I would like to thank Fei Wang and Min-Yu Huang for participating various collaborative projects with me. Both of them put great efforts into the projects, and their critical contributions are irreplaceable. I cherish my great memories with Sensen Li, Tso-Wei Li, and Doohwan Jung, for overnight tapeouts, luxury dinners, conference travels, and fun basketball games. I also want to thank other junior students and previous members in our group, Moez Aziz, Edgar Garay, Huy Thong Nguyen, Yeojoon Youn, Adam Wang, Sanghoon Lee, Tzu-Yuan Huang, Michael Kroger, Juan Pablo Caram Wigdorsky, Jun Luo, Bert Zhu, Choongsoon Kim, and Stefen Lepkowski for their support, and wish them great success in their future career.

Many of my research projects require expensive equipment for the measurements. I would like to thank Prof. John Cressler, Prof. Stephen Ralph, and GEDC for their generous support. I am indebted to Peter Song, Dr. Rob Schmid, Dr. Christopher Coen, Dr. Saeed Zeinolabedinzadeh, Dr. Wasif Khan, Dr. Ahmet Cagri Ulusoy, Dr. Pierre Isautier, and Jerrod Langston for many helpful discussions on high-frequency high-precision measurement techniques.

Our previous and current admins Lisa Salter, Carolyn Delay-Foster, and Maria Matheson have been extremely nice and helpful, especially when I need to make some last-minute orders. I am grateful for their assistance over the years.

My gratitude also goes to many other supportive friends at Georgia Tech, especially Bo Zhao, Di Chen, Xingjian Wang, Jiaming Li, Wenbin Wei, Dongdong Yao, Zefeng Li, Zhiyu Wang, Xujun Gu, Ye Han, Zhengkai Wu, Wenjing Su, Yunyi Gong, Jae Won Choi, Qi Fang, Zhen Wang, and Joe Gonzalez. I want to thank May Li and Lijun Zhu for being extremely nice and considerate as friends and roommates. I cherish our friendship and wish my friends all the best in the future.

My Ph.D. research has been supported by the Semiconductor Research Corporation (SRC), National Science Foundation (NSF), Defense Advanced Research Projects Agency (DARPA), Army Research Office (ARO), Analog Devices Inc., and Intel. I also want to acknowledge GlobalFoundries, IBM, and Toshiba for fabrication donation.

Finally and most importantly, I would like to thank my family for their unconditional love and support. My parents have been great role models in my life. Their wisdom, vision, enthusiasm, and work ethic have taught me to think deep and keep persistent. One of the greatest achievement in my life is to marry my beautiful wife Dr. Cai. She has always been encouraging and considerate. My Ph.D. research and dissertation would not have been possible without her support and companionship.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS AND ABBREVIATIONS

ACLR	Adjacent channel leakage ratio
ASK	Amplitude-shift keying
AWG	Arbitrary waveform generator
BER	Bit error rate
CMOS	Complementary metal-oxide semiconductor
CW	Continuous-wave
DPD	Digital predistortion
ED	Envelope detector
EHM	Even harmonic mixer
EIRP	Equivalent isotropically radiated power
EM	Electromagnetic
EVM	Error vector magnitude
FD	Full-duplex
IL	Injection locking
IoT	Internet-of-Things
Mm-wave	Millimeter-wave
OOK	On-off keying
PA	Power Amplifier
PCB	Printed circuit board
PS	Phase shifter
RF	Radio frequency
RTA	Reflection-type attenuator

RTPS	Reflection-type phase shifter
RX	Receiver
SI	Self-interference
SOI	Silicon-on-Insulator
SRF	Self-resonant frequency
SRR	Super-regenerative receiver
TDC	Time-to-digital converter
TDD	Time division duplex
T-line	Transmission line
THz	Terahertz
TX	Transmitter
VGA	Variable gain amplifier

SUMMARY

Millimeter-wave (mm-wave) and Terahertz (THz) frequency range is generally defined as frequencies between 30GHz to 3THz. With the recent advancement in mm-wave/THz technologies, it has shown great promise in a wide range of emerging applications, such as high-speed wireless communication, non-invasive imaging, biomedical sensing, non-destructive quality control, and spectroscopy. Until recently, mm-wave/THz systems have been mostly dominated by compound III-V processes and quasi-optical approaches. In this dissertation, we will present our design philosophies and approaches towards the development of fully integrated signal generation and detection systems for various emerging applications at mm-wave and THz using advanced silicon technologies.

First, a multi-feed antenna structure is proposed to realize direct on-antenna power combining with high efficiency. Based on this technique, a 60GHz on-chip linear radiator is demonstrated, achieving the highest output power among all the reported 60GHz power amplifiers (PAs) in silicon.

Secondly, by leveraging the concept of antenna-electronics co-design, a 60GHz full-duplex (FD) transceiver front-end with an on-chip multi-feed self-interference-canceling (SIC) antenna and an all-passive canceler is implemented. In our proof-of-concept demonstration, two FD TRX front-end chips are used to establish a 4Gb/s FD wireless link before using any digital-domain SIC, which is the first mm-wave FD link that supports Gb/s complex modulated signals simultaneously through the TX and RX.

Thirdly, a THz pico-radio concept is proposed and demonstrated to achieve extreme radio miniaturization at sub-millimeter scale. The proposed THz pico-radio concept will enable a wide variety of distributed sensing and Internet-of-Things applications, such as very-large-scale position/motion tracking, THz-range temperature/humidity monitoring, vibration/deformation sensing, and non-contact THz electromagnetic "tactile sensing".

Next, a multi-phase sub-harmonic injection locking technique is presented to enhance the system frequency tuning range for THz signal generation. Based on this technique, a scalable "active frequency multiplier" chain architecture and a multi-ring system topology are proposed to generate the desired THz signal from a low mm-wave frequency or RF reference source. We demonstrated a cascaded 3-stage 3-phase 2^{nd}-order sub-harmonic injection locking oscillator chain in an advanced silicon process, achieving the largest frequency tuning range (5.1%) and the best phase noise (-87dBc/Hz at 1MHz offset) among all the reported silicon-based THz oscillator sources at 0.5THz.

The last part of this dissertation introduces a full-band continuous-wave transceiver chipset for mm-wave/THz hyperspectral imaging. Hyperspectral imaging operates over a wide frequency range and offers spectroscopic information on each imaging pixel, which improves imaging sensitivity and specificity. Transmission mode hyperspectral images are successfully demonstrated at multiple frequencies in band for mm-wave/THz non-destructive evaluation and non-contact food safety screening applications.

CHAPTER 1. INTRODUCTION

"The best way to predict the future is to invent it."

— *Alan Kay*

Millimeter-wave (mm-wave) and Terahertz (THz) frequencies have recently stimulated an increasing research interest with their unique applications, such as spectroscopy, biomedical imaging, radar, and high-speed communication. One of the major technology roadblocks of applying mm-wave and THz technologies lies in the lack of low-cost, compact, energy efficient, and broadband signal generation and detection systems. Most existing mm-wave and THz radios are built based on discrete compound devices or quasi-optical approaches with low integration level and limited computational capabilities. On the other hand, the continuous device scaling in silicon technologies (CMOS or SiGe BiCMOS) has shown tremendous promise to realize self-contained mm-wave and THz systems with low cost and compact form-factor. This provides us with a powerful platform that supports a plethora of innovation opportunities both on the system level and circuit topology.

Taking full advantages of the increasing transistor speed, my Ph.D. research focuses on exploring new system architectures and circuit techniques to achieve state-of-the-art performance for various emerging applications at mm-wave and THz. Through my five-year Ph.D. study at Georgia Tech GEMS Lab, I have investigated the design challenges in mm-wave and THz transceivers, and devoted my research efforts in implementing high-power, energy efficient, and broadband signal generation and detection

systems using advanced silicon technologies. The important contributions of this dissertation are summarized below.

1. We propose a multi-feed antenna structure that synthesizes the desired far-field radiation characteristics with direct on-antenna power combining and increases the total radiated power of a wireless transmitter with high efficiency.
2. Based on the proposed multi-feed antenna, a 60GHz on-chip linear radiator is demonstrated, achieving the highest output power compared with the reported 60GHz power amplifiers (PAs) in silicon.
3. A 60GHz full-duplex (FD) transceiver front-end with an on-chip multi-feed self-interference-canceling (SIC) antenna and an all-passive canceler is implemented. In the system demonstration, two FD TRX chips are used to establish a 4Gb/s FD wireless link before using any digital-domain SIC, which is the first mm-wave FD link that supports Gb/s complex modulated signals simultaneously through the TX and RX. The proposed FD transceiver front-end also demonstrates the unique advantages of antenna-electronics co-design.
4. We perform the first exploratory study for designing Internet-of-Things (IoT) devices and "invisible" field-deployable sensor networks in THz frequencies to achieve sub-millimeter-scale form factor. A bidirectional low-power 320GHz pico-radio in CMOS is implemented and characterized.
5. A multi-phase sub-harmonic injection locking technique is proposed to increase the locking range of a multi-phase injection locking oscillator. By applying this technique, a 500GHz signal generation system is demonstrated which achieves

the largest frequency tuning range and the best phase noise among all the reported silicon-based THz oscillator sources at 0.5THz.

6. The first demonstration of an ultra-wideband transceiver chipset in silicon is presented for full-band continuous-wave mm-wave/THz hyperspectral imaging. The fully packaged wideband transceiver system offers a promising solution for low-cost field-deployable mm-wave/THz hyperspectral imaging.

The remainder of this dissertation is organized as follows.

Chapter 2 introduces the proposed multi-feed antenna for high-efficiency on-antenna power combining. A multi-feed slot antenna and a multi-feed square loop antenna are used as examples for theoretical study and experimental demonstration. The driving impedance for a multi-feed antenna is derived analytically, and circuit models based on ideal transformers are developed to describe its on-antenna power combining capability. The multi-feed slot antenna and multi-feed square loop antenna are implemented on the PCB at X-band, together with conventional single-feed antennas as reference designs. Measurement results are shown to verify the on-antenna power combining of the proposed multi-feed antennas. Furthermore, a 60GHz on-chip linear radiator as a 4-feed slot antenna driven by 16 unit PAs is presented, achieving the highest output power compared with the reported 60GHz PAs in silicon.

Chapter 3 presents a 60GHz transceiver front-end for full-duplex (FD) wireless communication. An on-chip multi-feed self-interference-canceling (SIC) antenna is proposed that naturally provides a high TX-RX isolation, an instantaneous broad bandwidth, and no additional TX/RX-path signal loss, in only one antenna footprint. An

all-passive zero-power RF canceler is also integrated on-chip with nearly orthogonal amplitude/phase tunability to further enhance SIC. Finally, two FD TRX front-end chips are used to demonstrate a 4Gb/s FD wireless link before using any digital-domain SIC.

Chapter 4 reports an exploratory study on using CMOS low-power THz radios to support high-quality short-range wireless links. A THz pico-radio concept is proposed that achieves extreme radio miniaturization to enable future "invisible" field-deployable sensor networks and IoT applications. The bidirectional TX/RX circuit sharing architecture is discussed in detail, and a low-power time-to-digital converter (TDC) is integrated on-chip to directly convert and digitize RX outputs. In addition, a high-quality wireless communication link based on OOK/M-ary ASK modulation is established between two THz pico-radio chips for system demonstration.

To increase the system frequency tuning range for broadband THz signal generation, a multi-phase sub-harmonic injection locking technique is proposed in Chapter 5. By applying this technique, a scalable "active frequency multiplier" chain architecture is proposed, which can generate a THz signal from a low mm-wave frequency or RF reference source. A multi-ring system topology is also proposed to implement this frequency multiplier scheme. We demonstrated a cascaded 3-stage 3-phase 2^{nd}-order sub-harmonic injection locking oscillator chain, which achieves the largest frequency tuning range and the best phase noise among all the reported silicon-based THz oscillator sources at 0.5THz.

In Chapter 6, a full-band continuous-wave hyperspectral imaging transceiver chipset is demonstrated. The imaging system comprises a 90-300GHz TX with a ±2dB

output power variation using a distributed quadrupler architecture and a 115-325GHz 4th subharmonic coherent RX with -115dBm sensitivity (1kHz RBW) using high-order filter-based matching networks. The TX and RX chips are flip-chip integrated with wideband Vivaldi antennas on LCP substrates to demonstrate transmission-mode imaging at multiple frequencies in-band for non-destructive evaluation and non-contact food safety screening applications.

Finally, Chapter 7 summarizes this dissertation.

CHAPTER 2. A MULTI-FEED ANTENNA FOR HIGH-EFFICIENCY DIRECT ON-ANTENNA POWER COMBINING

This chapter presents a multi-feed antenna structure that synthesizes the desired far-field radiation characteristics with on-antenna power combining and increases the total radiated power of a wireless transmitter. The driving signals at the multiple antenna feeds are scaled properly in amplitude and phase, so that they collectively synthesize the desired on-antenna current/voltage distribution and achieve the resulting desired far-field radiation pattern. The proposed multi-feed antenna offers flexibility to optimize the antenna driving impedances based on the locations of the feeds. It also simplifies the passive impedance-matching and power-combining networks between the antenna feeds and the transmitter outputs, substantially increasing the total transmitter power efficiency. Most importantly, the proposed multi-feed antenna achieves on-antenna low-loss power combining, which, compared with antenna-array based spatial power combining, does not suffer from narrowed beam-width or enlarged antenna panel size.

As proof of concept, multi-feed slot antennas and multi-feed square loop antennas are designed and characterized on PCB at 10.3GHz. Conventional single-feed slot antennas and single-feed square loop antennas are also implemented as reference designs. Well matched antenna gains and radiation patterns between the proposed multi-feed antennas and the conventional single-feed antennas are achieved in the measurements, demonstrating the on-antenna power combining of the proposed multi-feed antennas without distorting the far-field radiation patterns. An application example of a 60GHz on-

chip linear radiator is also presented in this chapter, which demonstrates the highest output power compared to any other reported silicon-based PA at 60GHz.

2.1 Introduction

Antennas are essential components in wireless systems that convert between electric signals and electromagnetic radiations [1]. Most existing antennas are single-feed radiators and pose fundamental challenges for the wireless transmitters that need to generate high radiated power from a limited supply voltage, such as base stations, mobile devices, and satellite transponders. In these applications, passive networks with large impedance transformation ratios are needed to down-transform the antenna impedance to the desired load-pull impedance of the high-power transmitters/power amplifiers (PAs) [2]–[4]. In practice, these passive networks with large impedance transformation ratios often experience high passive loss and limited bandwidth, directly degrading the transmitter power efficiency and limiting the operation frequency range [2]–[4].

To address this issue, power combining techniques are often required in these transmitter systems to generate large radiated power [5]–[29]. The existing power combining techniques can be generally divided into two categories. First, the outputs from multiple PAs can be combined at the single feed port of the antenna using passive power combining networks [5]–[18] [Figure 2.1(a)]. However, these lossy networks often degrade the total output power delivered to the antenna and lower the transmitter power efficiency. When the number of power combining units becomes larger, the power combining loss can even exceed the power combining gain, thus, adding more units results in diminishing returns.

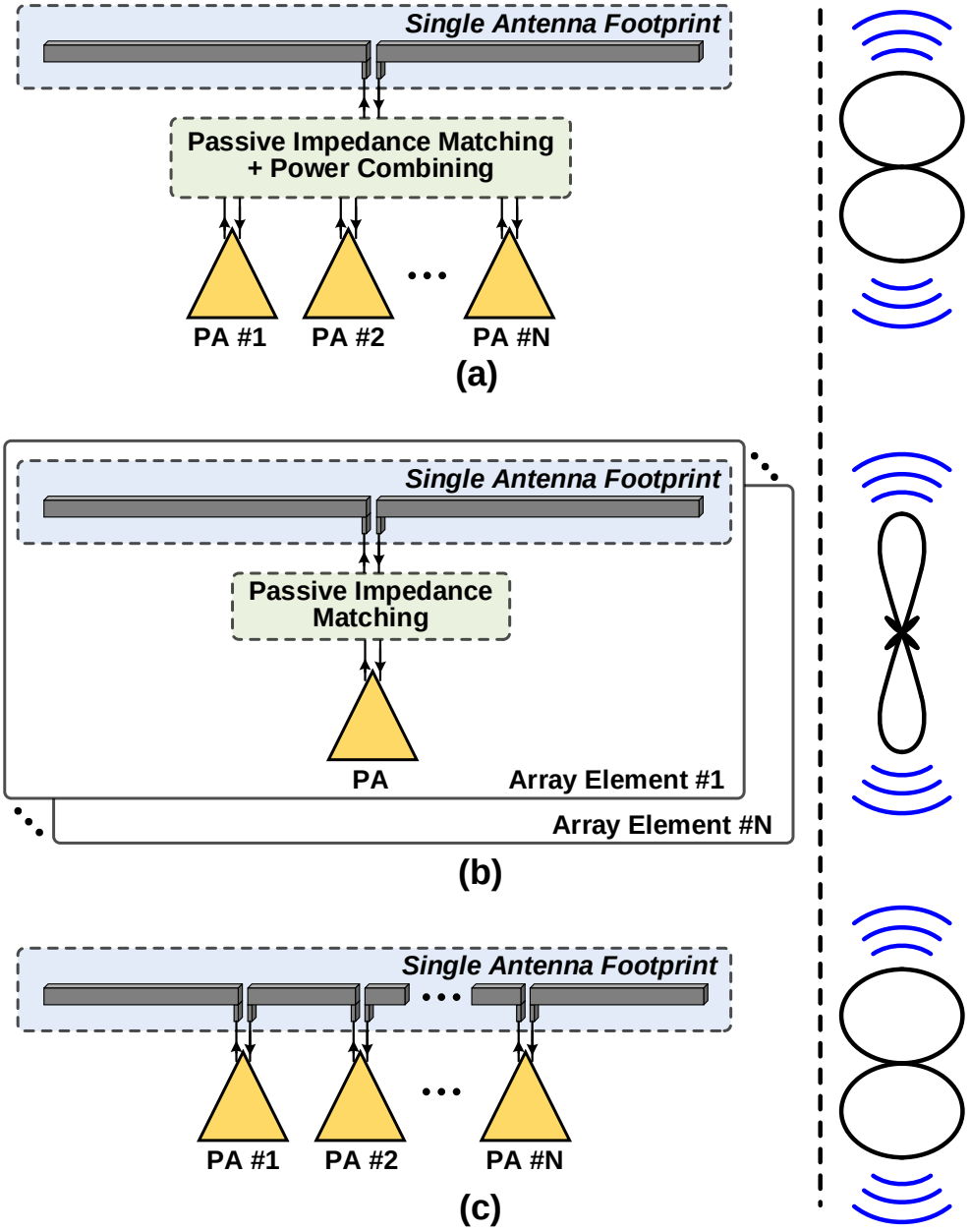

Figure 2.1 – (a) Power combining for a single-feed antenna using a passive network for impedance matching and power combining. (b) Array-based spatial power combining with conventional single-feed antennas. (c) Proposed multi-feed antenna for on-antenna power combining. The multi-feed antenna occupies only one antenna footprint and simplifies the passive networks at the PA outputs, substantially enhancing the transmitter output power and system power efficiency without sacrificing the beam-width or antenna panel size.

Antenna array based spatial power combining is an alternative solution to increase the total equivalent isotropically radiated power (EIRP) by combining the radiating E-/H-

field at the far-field [19]–[29] [Figure 2.1(b)]. However, it suffers from large array panel size. Moreover, an antenna array often presents a much narrower (or even pencil-sharp) beam-width, especially for large-scale antenna arrays. Such a narrow beam-width makes the alignment of the transmitter and receiver very challenging; it is particularly problematic for dynamic and mobile applications, such as mm-wave 5G wireless links [30] [31].

To address these challenges, we propose a multi-feed antenna structure that achieves low-loss on-antenna power combining to boost the total radiated power [32] [33] [Figure 2.1(c)]. The multi-feed concept has been demonstrated for mm-wave/THz signal generation [34]–[37]. Here, we want to explore its unique advantage for on-antenna power combining. The multiple antenna feeds are driven simultaneously, and the driving signals are scaled with proper amplitudes/phases which together actively synthesize the desired on-antenna RF current/voltage distribution, achieving the resulting desired far-field radiation pattern. Moreover, the multi-feed antenna constructively combines the power from each feed directly on the antenna, simplifying or even eliminating passive power combining networks. It also naturally achieves impedance down-scaling for transmitters without using extra passive matching networks, ensuring high system power efficiency. Furthermore, in contrast to the array-based spatial power combining technique, it is capable of boosting the total radiated power in only one antenna footprint and maintaining the field-of-view as a conventional single-feed antenna. In addition, the multi-feed antenna can be employed in an array to further increase the total radiated power.

Theoretically, the proposed direct on-antenna power combining concept using multiple concurrently driven antenna feeds can be applied to different antenna structures. Nevertheless, due to the limited space in this paper, we focus our theoretical study and

experimental demonstration on planar multi-feed slot and square loop antennas, both of which are popular antenna structures with a wide variety of applications. As proof-of-concept designs, one two-feed 0.5λ slot antenna, one three-feed 0.7λ slot antenna, and one two-feed 1λ square loop antenna are designed and characterized at X-band. X-band is widely used for radars and satellite communications [27] [38]. Note that the antenna input feeding networks are also implemented to facilitate the testing. These feeding networks can be eliminated in practice, since the proposed multi-feed antenna can be directly driven by multiple PAs/transmitters [39] [40]. A conventional single-feed 0.5λ slot antenna, a single-feed 0.7λ slot antenna, and a 1λ single-feed square loop antenna are implemented as reference designs for comparison.

This chapter is organized as follows. Section 2.2 introduces the proposed multi-feed 0.5λ slot antenna. A circuit model based on parallel-combing transformer is developed to describe its on-antenna power combining capability. Section 2.3 presents the proposed multi-feed 0.7λ slot antenna. A three-feed 0.7λ slot antenna is shown as a design example with detailed analysis on the antenna driving impedances. Section 2.4 discusses the proposed multi-feed 1λ square loop antenna. Measurement results of the multi-feed slot antenna and multi-feed square loop antenna on PCB are shown in Section 2.5 to compare the multi-feed antennas with the conventional single-feed antennas. Section 2.6 presents an application example of a 60GHz on-chip linear radiator, as a multi-feed antenna directly driven by multiple linear PAs, demonstrating the unique advantages of circuit-antenna co-designs.

2.2 Multi-Feed Half-Wavelength Slot Antenna

The radiation characteristics of an antenna, including the radiation pattern, beam-width, antenna gain, radiation efficiency, and polarization, are fully determined by the current/voltage distribution on the antenna [1]. For the proposed multi-feed half-wavelength (0.5λ) slot antenna, all the feeds are excited in the way that it exhibits the same voltage distribution as a conventional single-feed 0.5λ slot antenna, which leads to identical radiation characteristics of the two antennas. In parallel, the driving power from all the feeds are constructively combined on the multi-feed antenna, enabling on-antenna power combining without additional passive power combining networks.

To illustrate this concept, a two-feed 0.5λ slot antenna with symmetric feeding is studied first. Next, an asymmetric two-feed 0.5λ slot antenna and a general *N*-feed 0.5λ slot antenna are presented as extensions. 3D EM simulations using a 20mil Rogers® 3003 substrate (ε_r=3 and loss tangent tanδ=0.001) are carried at 10.3GHz operating frequency to verify the theory. Finally, a PCB design example of the symmetric two-feed 0.5λ slot antenna is shown with its input power distribution network. In practice, multiple PAs/transmitters can drive all the antenna feeds concurrently, and the input feeding network is eliminated [39] [40].

2.2.1 Two-Feed 0.5λ Slot Antenna with Symmetric Feeding

A conventional single-feed 0.5λ slot antenna at the operating frequency f_0 with its voltage distribution is shown in Figure 2.2(a). Assuming a narrow slot width (W=0.01λ), the voltage distribution on the slot is approximated as

$$V = V_0 \sin\left[k\left(\frac{L}{2} - |x|\right)\right] \text{ and } -\frac{L}{2} \le x \le +\frac{L}{2}, \tag{2.1}$$

where k is the wave number, L=0.5λ is the length of the slot, V_0 is the maximum voltage amplitude on the slot [1]. This distribution assumes that the voltage is zero at the two end points of the slot ($x = \pm L/2$).

Figure 2.2(b) shows a two-feed 0.5λ slot antenna with symmetric feeding. To match its voltage distribution with the conventional single-feed 0.5λ slot antenna [1], the relationship between the feeding location a and the normalized excitation voltage amplitude m is given as

$$m = \sin(2\pi a/\lambda). \tag{2.2}$$

With the identical voltage distribution on the slot antennas, the single-feed and the two-feed antennas radiate out the same power, as

$$\frac{{V_0}^2}{2R_{1\text{feed}}} = 2\frac{(mV_0)^2}{2R_{2\text{feed}}}, \tag{2.3}$$

where $R_{1\text{feed}}$ and $R_{2\text{feed}}$ are the real part of the driving impedance of the single-feed and two-feed 0.5λ slot antennas at f_0, respectively. (2.3) can be further simplified as

$$R_{2\text{feed}} = 2R_{1\text{feed}}\sin^2(2\pi a/\lambda) \tag{2.4}$$

The normalized driving impedance of the two-feed 0.5λ slot antenna is then derived as

$$R_{2\text{feed}}/R_{1\text{feed}} = 2\sin^2(2\pi a/\lambda) \tag{2.5}$$

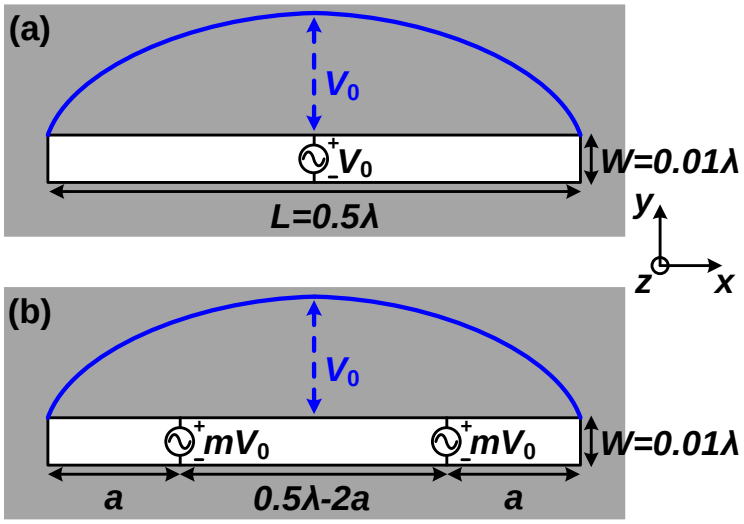

Figure 2.2 – (a) A conventional single-feed 0.5λ slot antenna at f_0 with its voltage distribution. (b) The proposed multi-feed 0.5λ slot antenna with two symmetric feeds as an example.

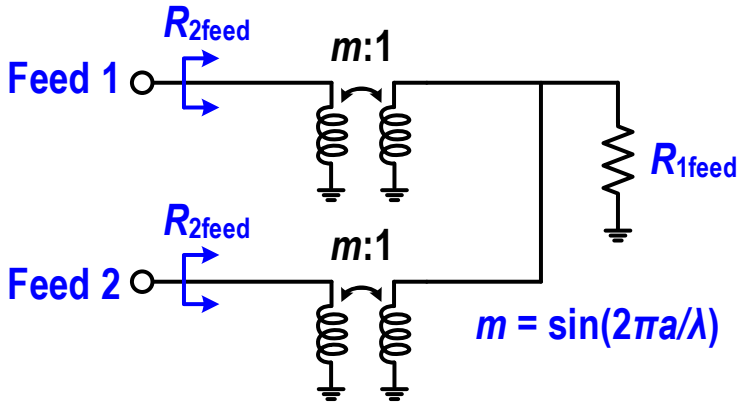

Figure 2.3 – Circuit model for the symmetric two-feed 0.5λ slot antenna at the resonance frequency f_0 based on parallel-combining transformers.

Based on (2.4) and (2.5), a circuit model for the symmetric two-feed 0.5λ slot antenna at the resonance frequency f_0 is developed (Figure 2.3). The circuit model is based on ideal parallel-combining transformers, and the turn ratio of the transformer is

$m = \sin(2\pi a/\lambda)$. The power from the feed 1 and feed 2 is in-phase combined and radiated out.

The theoretically calculated normalized driving impedance based on (2.5) and 3D EM-simulated normalized driving impedance at different feeding locations are plotted in Figure 2.4. Close agreement between the theoretical prediction and EM-simulation is achieved. One important feature of the symmetric two-feed 0.5λ slot antenna is that the normalized driving impedance is lower than 1 if the feeding location *a* is smaller than 0.125λ, meaning that the symmetric two-feed slot antenna down-scales the driving impedance compared to the single-feed antenna. This is particularly useful for the designs of high-power and efficient PA under a fixed voltage supply, which often require low optimum load-pull impedance [2]–[4]. By using a two-feed antenna, the passive impedance transformation network between the PA output and the antenna feed can be simplified or even eliminated; this reduces the loss and boosts the transmitter power efficiency. At the same time, the power from the two antenna feeds is in-phase combined on the antenna with low-loss.

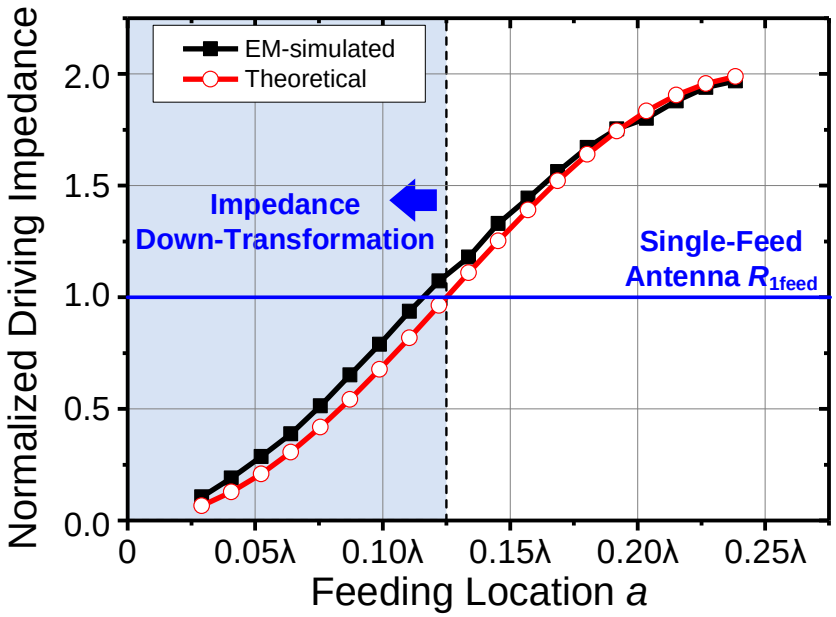

Figure 2.4 – Theoretically calculated and EM-simulated normalized driving impedances of the symmetric two-feed 0.5λ slot antenna versus the feeding location.

In practice, there may exist slight amplitude or phase mismatch between the two driving signals, especially when the two antenna feeds are driven by active electronics. In addition, due to the limited fabrication accuracy, there may also exist position mismatch between the two feeding locations. Figure 2.5 and Figure 2.6 summarize the effects of mismatches in a symmetric two-feed 0.5λ slot antenna, including the mismatches of feeding signal strength and feeding locations. By applying ±1dB amplitude mismatch between the feed 1 and feed 2 [Figure 2.5(b)], ±5° phase mismatch between the feed 1 and feed 2 [Figure 2.5(c)], and ±10% position mismatch of the feed 2 [Figure 2.6(b) and 2.6(c)], the EM-simulated voltage distribution on the slot, surface current (J_{surf}) distribution, and the E-/H-plane patterns are almost identical to that with perfect symmetric feeding signals, demonstrating the robustness of the symmetric two-feed 0.5λ slot antenna against driving signal mismatches.

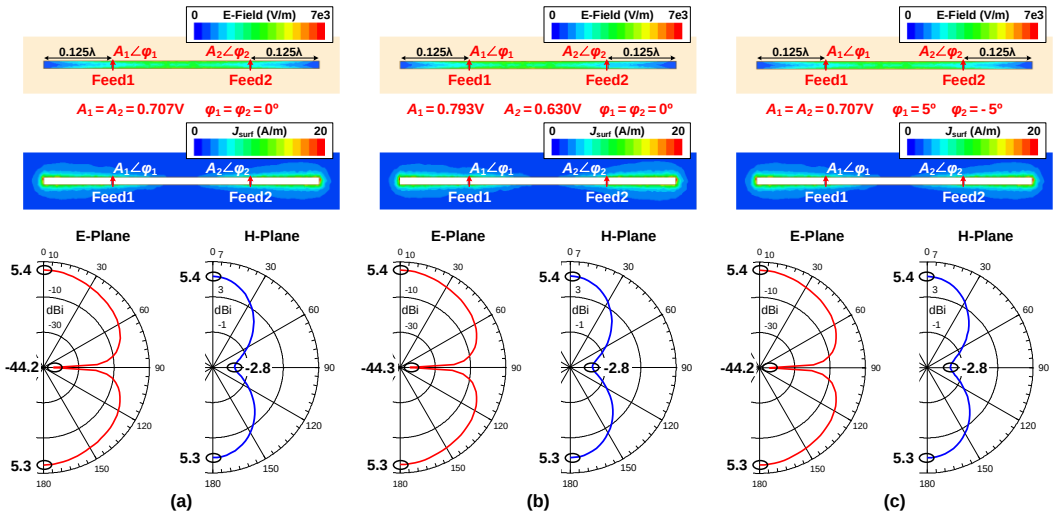

Figure 2.5 – EM-simulated voltage distribution on the slot, surface current (J_{surf}) distribution, and E-/H-plane patterns of the symmetric two-feed 0.5λ slot antenna with (a) symmetric driving, (b) ±1dB amplitude mismatch, and (c) ±5° phase mismatch.

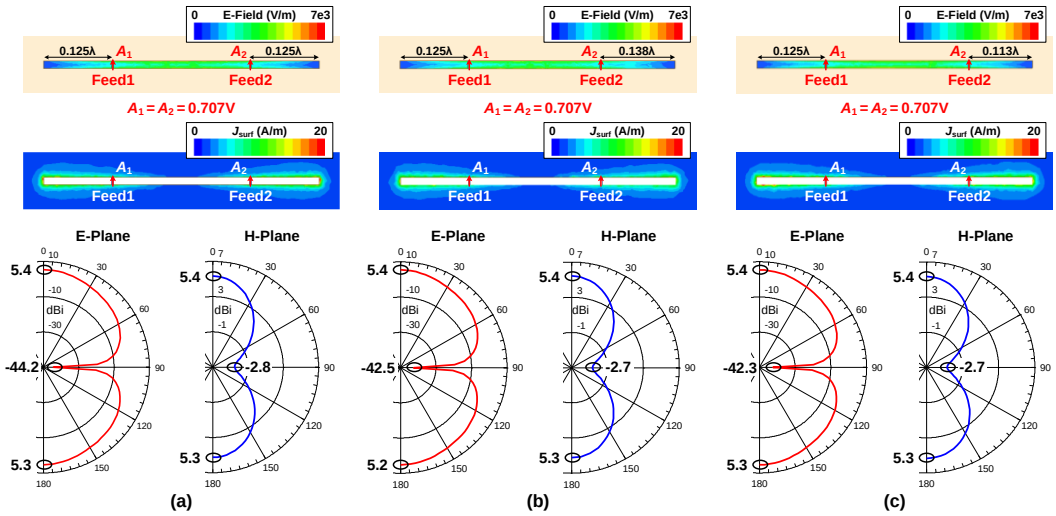

Figure 2.6 – EM-simulated voltage distribution on the slot, surface current (J_{surf}) distribution, and E-/H-plane patterns of the symmetric two-feed 0.5λ slot antenna with (a) symmetric driving, (b) +10% position mismatch of the feed 2, and (c) -10% position mismatch of the feed 2.

2.2.2 Asymmetric Two-Feed 0.5λ Slot Antenna

Similar to the symmetric two-feed 0.5λ slot antenna, two asymmetric feeds are placed on the 0.5λ slot antenna to mimic the voltage distribution of a conventional single-

feed 0.5λ slot antenna (Figure 2.7). The feed 1 is placed on the left side of the slot with a distance of *a* to the left end, while the feed 2 is placed on the right side of the slot with a distance of *b* to the right end. The relationship between the feeding location and the normalized excitation voltage amplitude is given as

$$m_1 = \sin(2\pi a/\lambda)\,, \qquad m_2 = \sin(2\pi b/\lambda)\,. \tag{2.6}$$

The total radiated power of this asymmetric two-feed antenna is the same as a conventional single-feed 0.5λ slot antenna, as

$$\frac{{V_0}^2}{2R_{1\text{feed}}} = \frac{(m_1 V_0)^2}{2R_{2\text{feed}_1}} + \frac{(m_2 V_0)^2}{2R_{2\text{feed}_2}}, \tag{2.7}$$

where $R_{2\text{feed}_1}$ and $R_{2\text{feed}_2}$ are the real part of the driving impedances of the two asymmetric feeds at f_0, respectively. (2.7) can be further simplified as

$$R_{1\text{feed}} = \frac{R_{2\text{feed}_1}}{{m_1}^2} // \frac{R_{2\text{feed}_2}}{{m_2}^2}, \tag{2.8}$$

which can be modeled using an equivalent parallel-combining circuit model with transformer scaling shown in Figure 2.8.

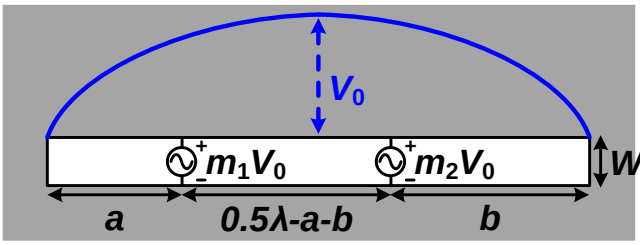

Figure 2.7 – The proposed multi-feed 0.5λ slot antenna with two asymmetric feeds.

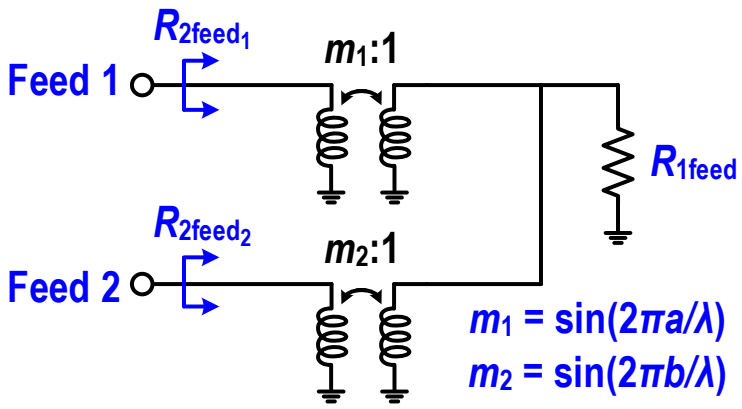

Figure 2.8 – Circuit model for the asymmetric two-feed 0.5λ slot antenna at the resonance frequency f_0 based on parallel-combining transformers.

EM simulations are performed to verify the voltage distribution and radiation patterns of the asymmetric two-feed 0.5λ slot antennas (Figure 2.9). In the simulations, the feed 1 is fixed at the center of the left side (a=0.125λ), while the feed 2 is placed at three different locations (b=0.25λ, 0.167λ, 0.083 λ). The EM-simulated E-/H-plane patterns are almost identical as the single-feed and symmetric two-feed 0.5λ slot antennas. These results show that asymmetric two-feed 0.5λ slot antenna can still achieve constructive on-antenna power combining and the desired radiation pattern, as long as their input signals are scaled accordingly to the feed locations.

However, compared with symmetric two-feed 0.5λ slot antenna, the asymmetric design often requires two sets of PAs/transmitters in practice due to the imbalance of the driving impedances $R_{2\text{feed}_1}$ and $R_{2\text{feed}_2}$, thus, adding complexity to the designs of PA/transmitter and input power distribution network.

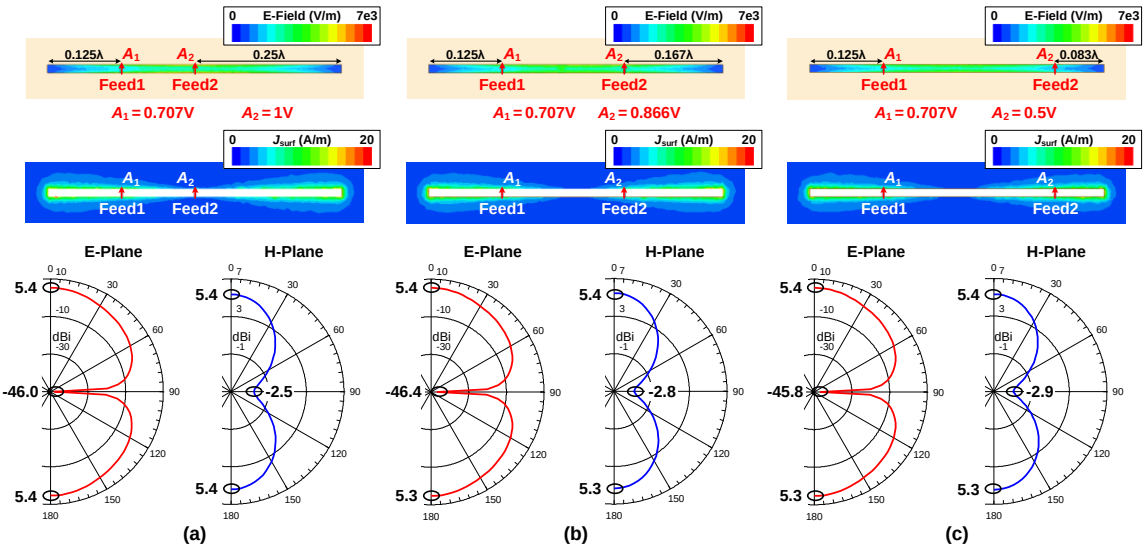

Figure 2.9 – EM-simulated voltage distribution on the slot, surface current (J_{surf}) distribution, and E-/H-plane patterns of the asymmetric two-feed 0.5λ slot antenna with (a) b=0.25λ, (b) b=0.167λ, and (c) b=0.0.83λ. The feed 1 is fixed at the center of the left side (a=0.125λ) for all the EM simulations.

2.2.3 General N-Feed 0.5λ Slot Antenna

The number of antenna feeds can be increased to N as an extension of the asymmetric two-feed 0.5λ slot antenna (Figure 2.10).

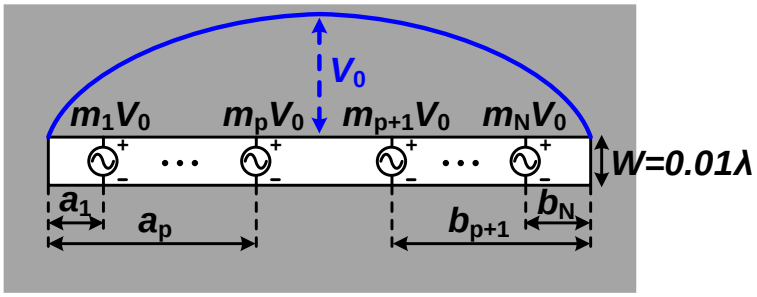

Figure 2.10 – The proposed multi-feed 0.5λ slot antenna with N feeds.

The relationship between the feeding location and the normalized excitation voltage amplitude is given as

$$m_{\mathrm{k}} = \sin(2\pi a_{\mathrm{k}}/\lambda) \qquad \text{for } 1 \le k \le p,$$
$$m_{\mathrm{k}} = \sin(2\pi b_{\mathrm{k}}/\lambda) \quad \text{for } p+1 \le k \le N, \tag{2.9}$$

There is no theoretical limitation on how many antenna feeds can be used. Nevertheless, adding more feeds presents several practical limitations. First, in asymmetric feeding cases, each antenna feed at different location normally has different driving impedance. Therefore, the PA/transmitter and the input power distribution networks need to be customized for each feed impedance, so that all the antenna feeds are driven in a high-efficiency and constructive fashion; this will add system complexity and cost. In addition, the physical size of the electronics, i.e., the PA/transmitter and the matching networks, also limit the number of feeds that can be concurrently driven in practice.

2.2.4 A PCB Design Example of the Symmetric Two-Feed 0.5λ Slot Antenna

A prototype design of the symmetric two-feed 0.5λ slot antenna with a=0.125λ is selected for demonstration [Figure 2.11(a)] [32]. The driving voltages at the two feeds have the same amplitudes and phases due to symmetry. A 1:2 parallel power divider and matching network are thus designed to drive the two antenna feeds and enable the testing. A Y-junction first splits the input 50Ω transmission line (T-line) to two parallel 100Ω T-lines [Figure 2.11(a)]. Next, a two-section λ/4 impedance transformer matches the 100Ω T-line to the driving impedance of the two-feed antenna. In this design, one 140Ω λ/4 impedance transformer is followed by another 48Ω λ/4 impedance transformer. Grounded co-planar waveguides (GCPW) are used to suppress the radiation of the feeding network [41]. The simulated peak antenna gain is 4.97dBi with a simulated radiation efficiency of

87% at 10.4GHz. A conventional single-feed 0.5λ slot antenna is designed as a reference [Figure 2.11(b)] with a simulated peak antenna gain of 4.57dBi and a simulated radiation efficiency of 89%. In these 3D EM simulations, closely matched patterns and radiation efficiencies are achieved for the proposed two-feed and conventional single-feed 0.5λ slot antennas.

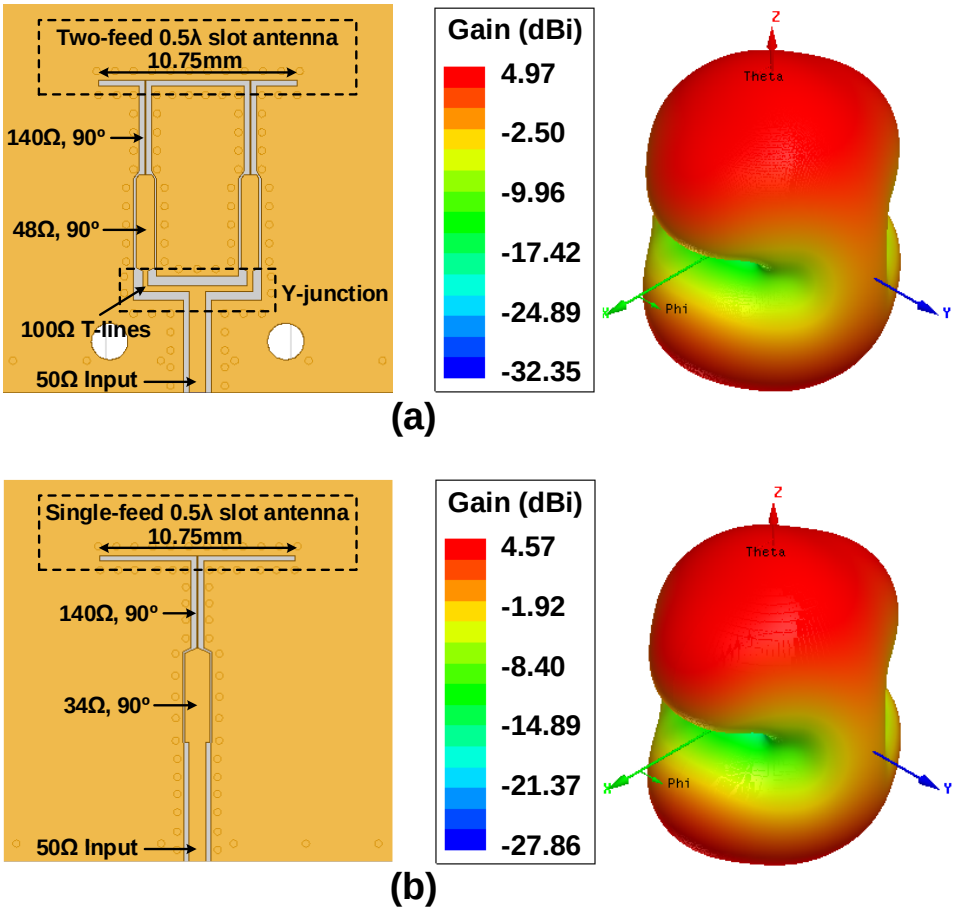

Figure 2.11 – (a) The 3D EM model of the symmetric two-feed 0.5λ slot antenna with the input feeding network and its simulated 3D radiation pattern. (b) The 3D EM model of the single-feed 0.5λ slot antenna and its simulated 3D radiation pattern.

2.3 Multi-Feed Non-Resonant Slot Antenna

In this section, the length of the slot L is increased above 0.5λ to show the generality of the multi-feed slot antenna. A design example based on three antenna feeds with L=0.7λ using a 20mil Rogers® 3003 substrate (ε_r=3 and loss tangent tanδ=0.001) is discussed and EM-simulated.

The 3-feed slot antenna is shown in Figure 2.12. The feed 1 and feed 3 are symmetrically placed on the slot, while the feed 2 is put on the center of the slot. The three feeds are driven in-phase with the voltage amplitude of nV_0, rV_0, and nV_0.

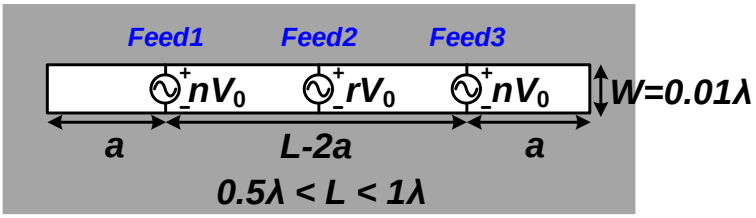

Figure 2.12 – The proposed multi-feed slot antenna with a three-feed slot antenna as an example.

The driving impedances of the three-feed slot antenna are important parameters when designing the antenna together with PAs/transmitters. To derive the driving impedances at f_0, the three-feed slot antenna is modeled as a three-port passive network. The holistic behavior of a multi-feed passive network is determined by its driving conditions of all the ports, because of the active pulling effects among the ports (i.e., finite isolation) [42]. With the voltage excitations applied on the slot antenna, it is convenient to use the admittance matrix [Y] to model the three-feed slot antenna, as

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} \tag{2.10}$$

where V_1, V_2, and V_3 are the three driving voltages at the three antenna feeds. The matrix entry Y_{ij} can be determined by driving the port j with the voltage V_j, short-circuiting all the other ports (V_k=0 for $k \neq j$), and measuring the short-circuit current at the port i as

$$Y_{ij} = \frac{I_i}{V_j} \tag{2.11}$$

Thus, the complete [Y] matrix can be determined.

Due to symmetry and reciprocity of the three-feed antenna structure, there are four independent entries in the 3×3 [Y] matrix, i.e., Y_{11}, Y_{12}, Y_{13}, and Y_{22}. These four entries are solved as follows.

First, only the feed 1 is excited, while the feed 2 and feed 3 are shorted [Figure 2.13(a)]. When a is small, i.e., the feed 1 and feed 3 are far away from each other, the feed 3 is bypassed by the short-circuited feed 2, giving

$$Y_{13} \approx 0 \tag{2.12}$$

This is verified by the 3D EM-simulated E-field distribution on the slot [Figure 2.13(b)] and the EM-simulated surface current (J_{surf}) distribution [Figure 2.13(c)]. In this simulation, L is chosen as 0.7λ and a is chosen as 0.15λ. Negligible E-field is presented at the feed 3, and little current flows through the feed 3 compared with the feed 1 and feed 2.

With the above approximation, the feed 1 is essentially the feed of an off-center-fed single-feed slot antenna with a length of $L/2$, and the distance between the feed 1 and left end of the slot is a. Its input admittance (Y_{11}) can be close-form derived [43] [44] or numerically calculated [45]. Here, 3D EM simulation is used to extract its value. Similarly, Y_{12} can be extracted by using 3D EM simulation.

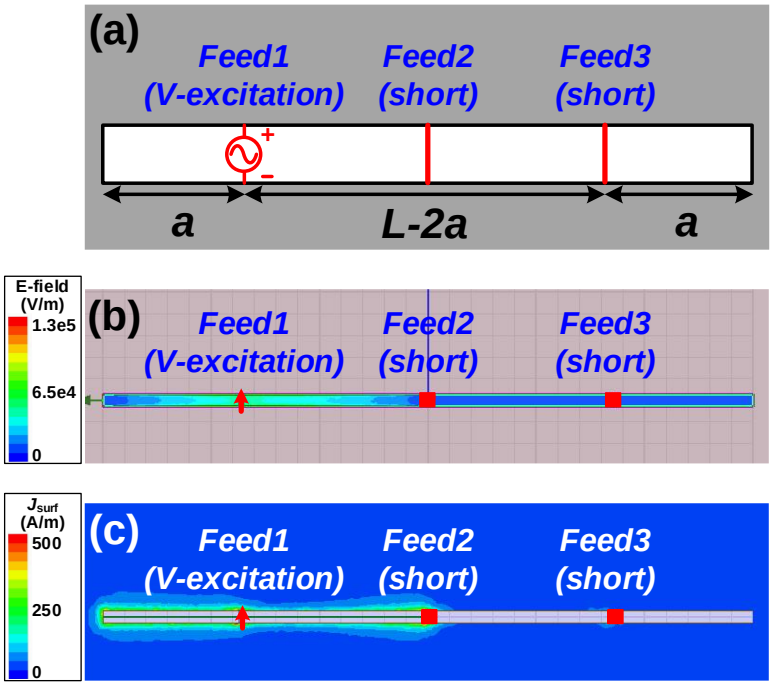

Figure 2.13 – (a) Feed 1 is driven by a voltage source, while the feed 2 and feed 3 are shorted to determine Y_{11}, Y_{12}, and Y_{13} in the 3-feed slot antenna [Y] matrix. 3D EM-simulated (b) E-field distribution and (c) surface current (J_{surf}) distribution on the slot by applying the driving/boundary conditions in (a). In the EM simulations, L=0.7λ and a=0.15λ.

Note that the assumption $Y_{13} \approx 0$ may not hold when a becomes larger, i.e., the feed 1 and feed 3 are closer, due to the stronger coupling between feed 1 and feed 3. Therefore, 3D EM simulation is also performed to accurately extract Y_{13} for different feeding locations. The 3D EM-simulated Y_{11}, Y_{12} and Y_{13} versus the feeding location a are plotted in Figure 2.14 for L=0.7λ. The results verify that $Y_{13} \approx 0$ is valid for a < 0.2 λ.

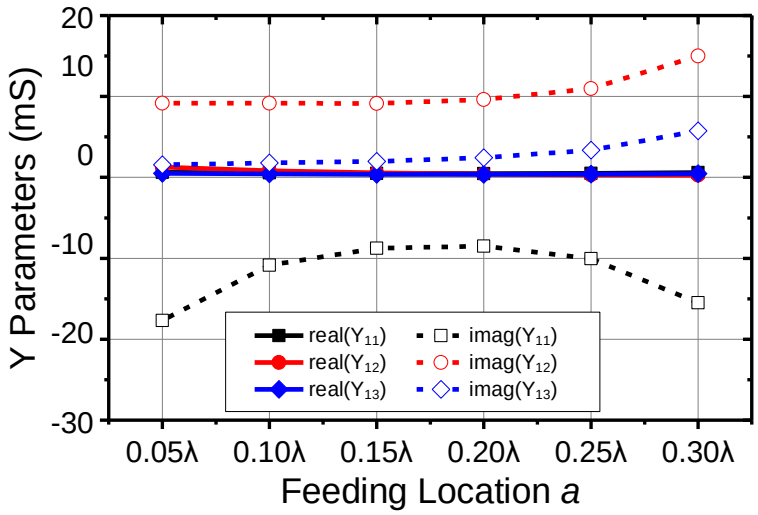

Figure 2.14 – 3D EM-simulated Y_{11}, Y_{12}, and Y_{13} versus the feeding location a for a three-feed slot antenna with L=0.7λ at f_0.

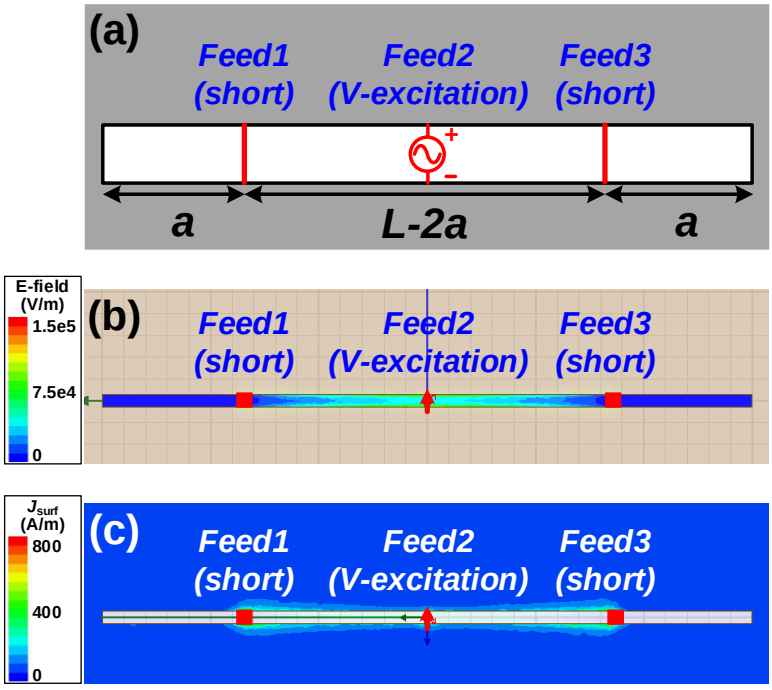

Figure 2.15 – (a) Feed 2 is driven by a voltage source while the feed 1 and feed 3 are shorted to determine Y_{22} in the 3-feed slot antenna [Y] matrix. 3D EM-simulated (b) E-field distribution and (c) surface current distribution on the slot by applying the driving/boundary conditions in (a). In the EM simulations, L=0.7λ and a=0.15λ.

Next, only the feed 2 of the multi-feed antenna is excited while the feed 1 and feed 3 are shorted (Figure 2.15). The feed 2 is then approximated as a center-fed single-feed slot

antenna with a length of (L-2a). Its input admittance (Y_{22}) can be close-form derived [43] [44] or numerically calculated [45]. The 3D EM-simulated Y_{22} versus the feeding location is shown in Figure 2.16 assuming L=0.7λ. Y_{22} is capacitive when (L-2a) > 0.5λ and becomes inductive when (L-2a) < 0.5λ. This matches the driving impedance behavior of a single-feed slot antenna.

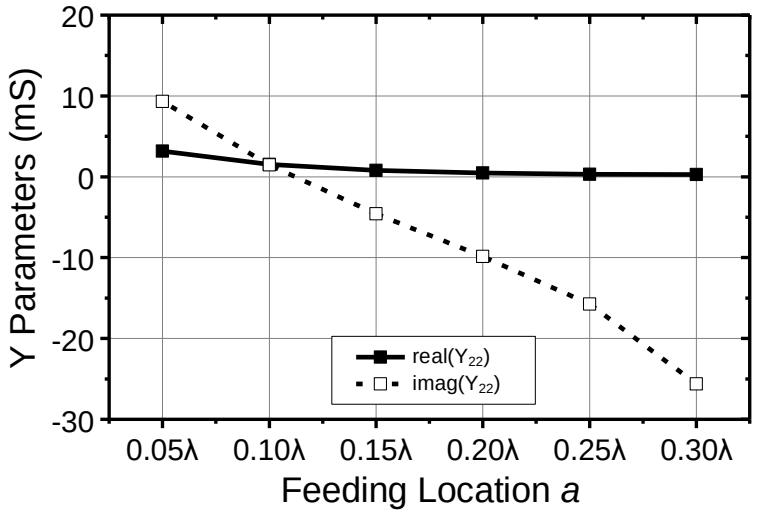

Figure 2.16 – 3D EM-simulated Y_{22} versus the feeding location for a three-feed slot antenna with L=0.7λ at f_0.

Once the [Y] matrix is determined, the driving impedances of the three-feed antenna are obtained by applying three excitations at the three antenna feeds. In our case, the three feeds are driven in-phase with the voltage sources nV_0, rV_0, and nV_0. The voltage amplitude is defined as

$$n = \sin(2\pi a/\lambda), \qquad r = \sin(2\pi L/\lambda). \tag{2.13}$$

Thus, the driving impedances are

$$Z_{3\text{feed}_1} = Z_{3\text{feed}_3} = \frac{V_1}{I_1} = \frac{n}{nY_{11} + rY_{12} + nY_{13}} \tag{2.14}$$

$$Z_{3\text{feed}_2} = \frac{V_2}{I_2} = \frac{r}{nY_{21} + rY_{22} + nY_{23}} \tag{2.15}$$

where $Z_{3\text{feed}_1}$ (or $Z_{3\text{feed}_3}$) is the driving impedance of the feed on the side, and $Z_{3\text{feed}_2}$ is the driving impedance of the center feed, when the three feeds are excited simultaneously. Using the [Y] matrix obtained by the 3D EM-simulations, the parallel impedance of $Z_{3\text{feed}_1}$ and $Z_{3\text{feed}_2}$ at f_0 are calculated and plotted in Figure 2.17, assuming L=0.7λ. Both $Z_{3\text{feed}_1}$ and $Z_{3\text{feed}_2}$ are capacitive for all the feeding locations.

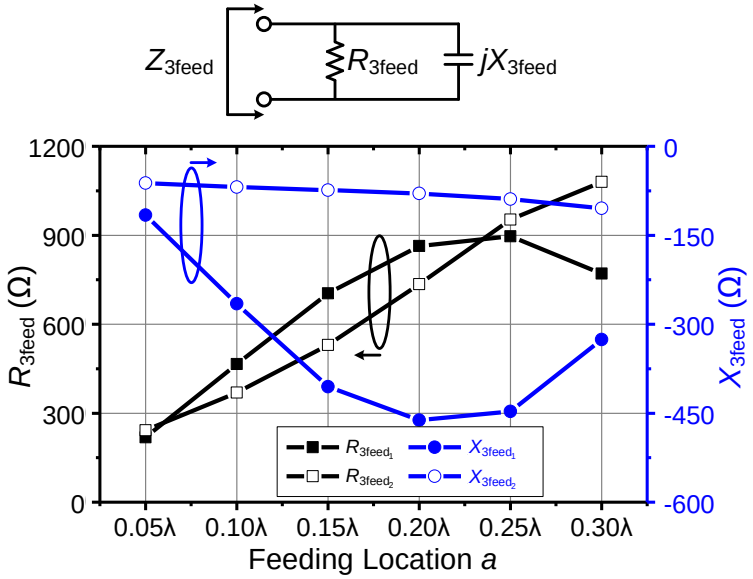

Figure 2.17 – Driving impedances of the three feeds versus the feeding location *a* for a three-feed slot antenna with *L*=0.7λ at f_0, when all the three feeds are driven in-phase with the voltage sources nV_0, rV_0, and nV_0. $Z_{3\text{feed}_1} = R_{3\text{feed}_1}//jX_{3\text{feed}_1}$ (or $Z_{3\text{feed}_3} = R_{3\text{feed}_3}//jX_{3\text{feed}_3}$) is the driving impedance of the feed on the side, and $Z_{3\text{feed}_2} = R_{3\text{feed}_2}//jX_{3\text{feed}_2}$ is the driving impedance of the center feed.

A prototype design of the three-feed 0.7λ slot antenna is shown in Figure 2.18 [32]. The feeding location a is chosen as 0.175λ so that the input power at all the three feeds are

the same to ease the input feeding network design. Therefore, these three feeds are driven by an equal-power 1:3 divider. The driving impedances of the center feed and the feeds on the side are 677Ω//210fF and 821Ω//30fF, respectively. These driving impedances are first matched to 150Ω by double-stub and single-stub matching circuits [42]. The equivalent schematics of the matching networks are shown in Figure 2.19. Then, additional 150Ω meander lines are used to ensure that the phases of the driven voltages at the three antenna feeds are the same. Next, the three 150Ω T-lines are combined in parallel and merged to the input 50Ω T-line (Figure 2.18). The 3D EM-simulated radiation efficiency including the feeding network is 87% with a simulated peak antenna gain of 4.58dBi at 10.3GHz. A conventional single-feed 0.7λ slot antenna is designed as a reference with a simulated peak antenna gain of 5.1dBi and a simulated radiation efficiency of 90% at 10.1GHz.

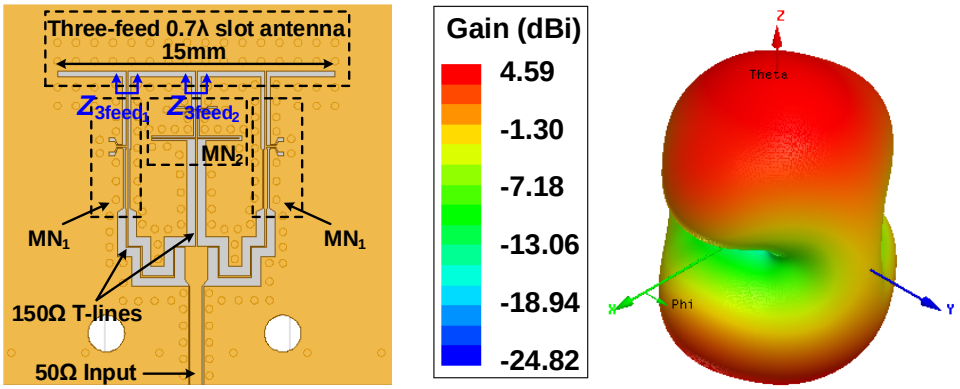

Figure 2.18 – The 3D EM model of the three-feed 0.7λ slot antenna with the input feeding network and its simulated 3D radiation pattern.

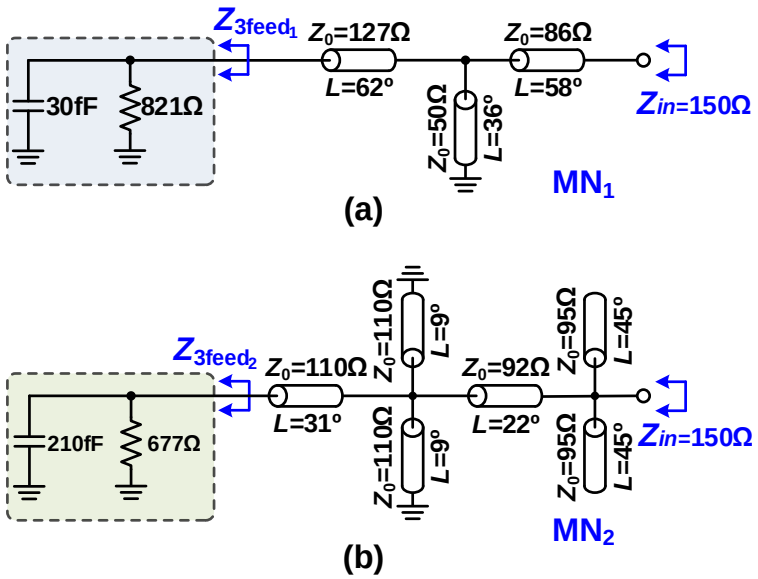

Figure 2.19 – Equivalent circuit schematics of the matching networks for the three-feed 0.7λ slot antenna.

2.4 Multi-Feed Square Loop Antenna

The proposed multi-feed antenna concept can be extended to other antenna structures and for on-antenna power combining and impedance scaling. In this section, a multi-feed 1λ square loop antenna is presented and compared with a conventional single-feed 1λ square loop antenna.

The 1λ square loop antenna has 1/4λ-length on each side, and the current distribution is approximated as sinusoidal [46] [47]. The conventional single-feed 1λ square loop antenna and its current distribution at the operation frequency f_0 are shown in Figure 2.20(a). The current maxima happen at the antenna feed and the center of the opposite side of the loop. The current nulls locate at the center of two sides perpendicular to the feed side. The amplitude of the maximum current is assumed to be I_0.

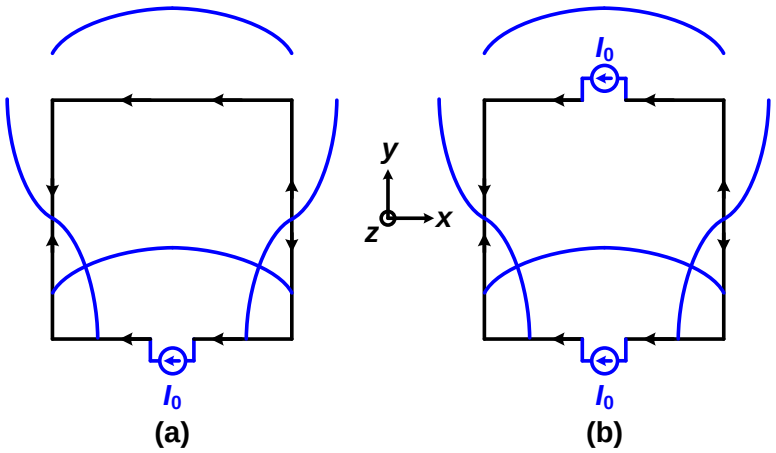

Figure 2.20 – (a) The single-feed 1λ square loop antenna with its current distribution at f_0. (b) The two-feed 1λ square loop antenna with its current distribution at f_0.

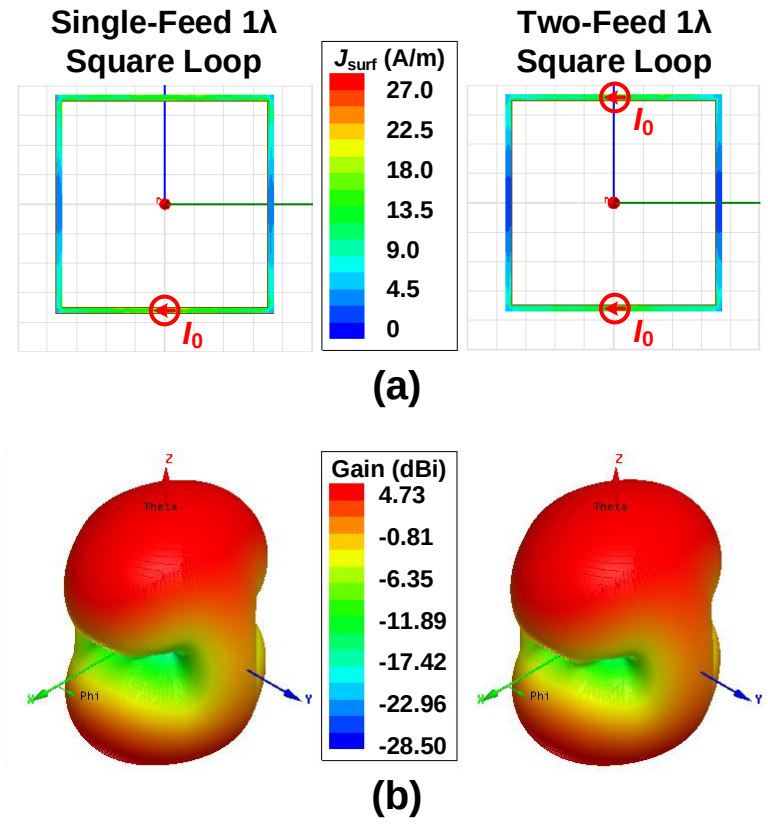

Figure 2.21 – (a) The 3D EM-simulated surface current distributions (J_{surf}) of the single-feed and two-feed 1λ square loop antennas at 10.3GHz. (b) The 3D EM-simulated 3D radiation patterns of the single-feed and two-feed 1λ square loop antennas at 10.3GHz.

In the proposed two-feed 1λ square loop antenna [Figure 2.20(b)], a second feed is added at the other current maximum with the equal current amplitude of I_0. Due to the symmetry, the two-feed 1λ square loop antenna achieves the identical current distribution as the single-feed 1λ square loop antenna, and thus generates the same far-field radiation pattern.

The proposed two-feed 1λ square loop antenna is verified using 3D EM simulations. The single-feed and two-feed 1λ square loop antennas are designed on a 10mil-thick Rogers® 3003 substrate at 10.3GHz. The total loop length is 28mm. The 3D EM-simulated surface current distributions and the far-field radiation patterns of the two antennas are shown in Figure 2.21. A close match is achieved in the 3D EM simulations, verifying that the proposed two-feed 1λ square loop antenna synthesizes the identical current distribution and radiation pattern as its single-feed counterpart. At the same time, the power from the two feeds are efficiently combined on the antenna, achieving on-antenna power combining without additional passive power combining networks.

Similar to the two-feed 0.5λ slot antenna presented in the Section 2.2, the driving impedance of the two-feed square loop antenna is derived by equating the total radiated power from the single-feed and the two-feed square loop antennas, as

$$\frac{{I_0}^2 R_{1\text{feed}}}{2} = 2\frac{{I_0}^2 R_{2\text{feed}}}{2}, \tag{2.16}$$

where $R_{1\text{feed}}$ is the radiation resistance of the single-feed square loop antenna, and $R_{2\text{feed}}$ is the driving impedance of each feed in the two-feed square loop antenna. Equation (2.16) is further simplified as

$$R_{2\text{feed}} = R_{1\text{feed}}/2 \tag{2.17}$$

The driving impedance of the two-feed square loop antenna ($R_{2\text{feed}}$) is only half of the radiation resistance of the single-feed square loop antenna ($R_{1\text{feed}}$). This inherent impedance down-transformation by a factor of 2 is particularly beneficial for the antenna to interface with high-power and high-efficiency PAs [2]–[4].

The 3D EM-simulated $R_{1\text{feed}}$ and $R_{2\text{feed}}$ versus frequency are plotted in Figure 2.22. The single-feed square loop antenna resonates at 10.8GHz with a radiation resistance of 197Ω, while the two-feed square loop antenna resonates at 10.4GHz with a driving impedance of 95Ω, verifying the impedance down-transformation by a factor of 2.

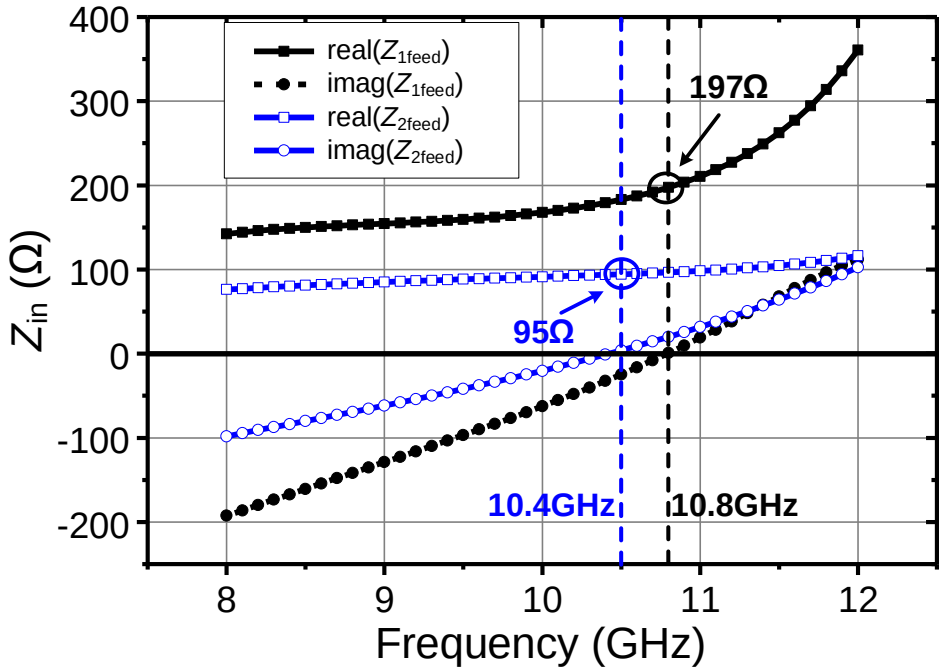

Figure 2.22 – The simulated driving impedances of the single-feed and two-feed 1λ square loop antennas versus frequency.

For the testing purpose, a 1:2 power divider and input matching network is designed to drive the two antenna feeds. The 3D EM model of the two-feed 1λ square loop antenna and its simulated 3D radiation pattern are shown in Figure 2.23. For the 1:2 power divider and matching network, a Y-junction is first splits the input 50Ω transmission line (T-line) to two parallel 100Ω T-lines. Next, a delay-line based balun is used to generate differential feed signals and match the 100Ω T-line to the differential feed of the two-feed antenna. The simulated peak antenna gain is 4.53dBi with a simulated radiation efficiency of 93% at 10.3GHz.

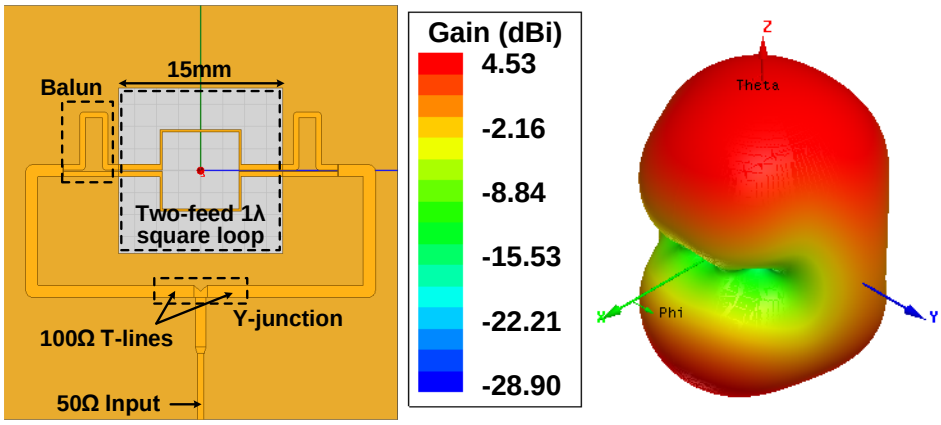

Figure 2.23 – The 3D EM model of the two-feed 1λ square loop antenna with the input feeding network and its simulated 3D radiation pattern.

The multi-feed square loop antenna concept can also be extended with more feeds. For example, a four-feed 1λ square loop antenna example is shown in Figure 2.24(b). The four feeds locate at the four corners of the square loop with an excitation current amplitude of $I_0/\sqrt{2}$. It achieves the same current distribution on the antenna as the single-feed square loop antenna, and thus, generates the same far-field radiation pattern. The power from the four antenna feeds are also efficiently combined on the antenna with low loss.

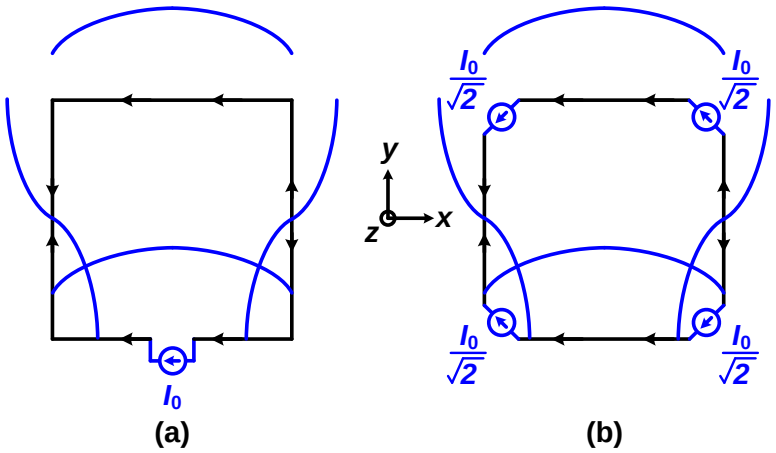

Figure 2.24 – (a) The single-feed 1λ square loop antenna with its current distribution at f_0. (b) A proposed four-feed 1λ square loop antenna with its current distribution at f_0.

2.5 Measurement Results of the Multi-Feed Antennas on PCB

To experimentally verify the proposed multi-feed antenna concept for on-antenna power combining, a two-feed 0.5λ slot antenna, a three-feed 0.7λ slot antenna, and a two-feed 1λ square loop antenna are fabricated and measured. A single-feed 0.5λ slot antenna, a single-feed 0.7λ slot antenna, and a single-feed 1λ square loop antenna are also implemented as reference designs. The photographs of the fabricated antenna prototypes are shown in Figure 2.25. The measurement was performed using an R&S VNA (ZVA24) with a distance of 66cm between a standard X-band horn antenna and the antenna under test to ensure far-field characterizations.

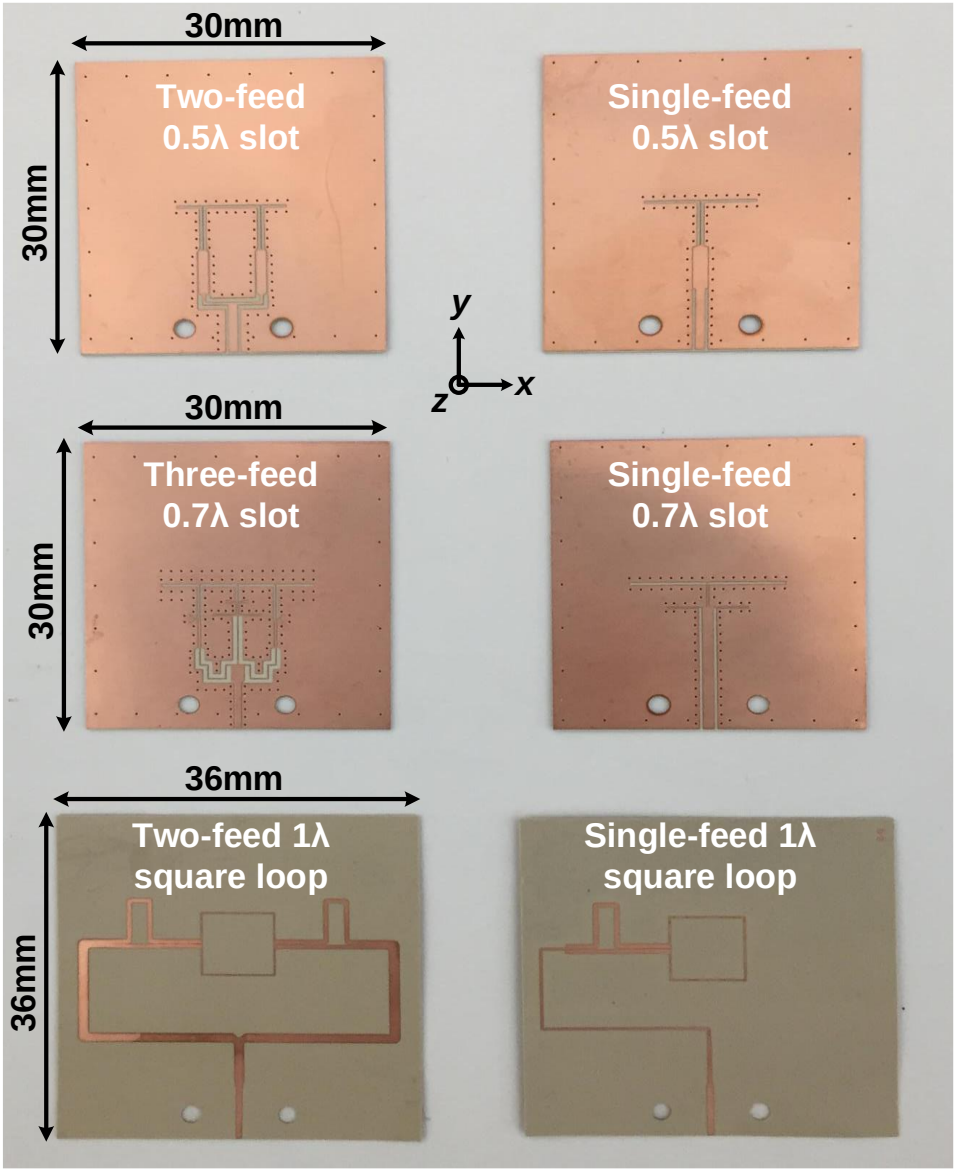

Figure 2.25 – Photographs of the fabricated antenna samples using Rogers® 3003 substrate (ε_r=3 and tanδ=0.001). The slot antennas use 20mil-thick substrate, while the square loop antennas use 10mil-thick substrate.

2.5.1 Input Matching and Peak Antenna Gain Measurements

The measured return loss versus the operating frequency of the antenna samples are summarized in Figure 2.26. The two-feed 0.5λ slot antenna achieves its input matching bandwidth (return loss < -10dB) from 10.2GHz to 10.55GHz, while the single-feed 0.5λ reference design has the input matching bandwidth from 10.45GHz to 10.85GHz [Figure

2.26(a)]. Similarly, the three-feed 0.7λ slot antenna achieves its input matching bandwidth from 9.95GHz to 10.5GHz, while the single-feed 0.7λ reference design has the input matching bandwidth from 9.85GHz to 10.35GHz [Figure 2.26(b)]. Both measurements show well matched bandwidth for the multi-feed and single-feed slot antennas. The relatively narrow bandwidths of these slot antennas are mainly determined by the inherent antenna structure. In practical implementations, the multi-feed antennas can be co-designed and integrated with PAs/transmitters to minimize the matching networks in-between and allow for the best use of the antenna bandwidth. Therefore, the antenna bandwidth is not fundamentally limited by the proposed multi-feed concept. On the other hand, the square loop antenna has a much larger input matching bandwidth compared with slot antennas. The input matching bandwidth of the two-feed 1λ square loop antenna is from 9.55GHz to 11.3GHz (16.8%), shown in Figure 2.26(c), also matching well with the single-feed 1λ square loop antenna (9.3GHz to 11.3GHz with 19.4%).

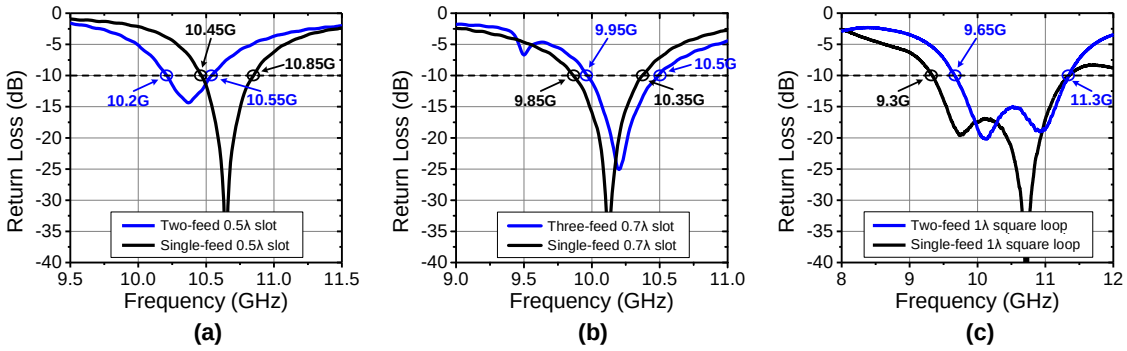

Figure 2.26 – Measured return losses for (a) two-feed and single-feed 0.5λ slot antenna, (b) three-feed and single-feed 0.7λ slot antenna, and (c) two-feed and single-feed 1λ square loop antenna.

The peak antenna gains locate at the boresight for all the samples. Figure 2.27 summarizes the measured peak antenna gains versus the operating frequency. The peak antenna gains of all the samples at their center frequencies are between 4.7 and 5.0dBi,

matching well with the 3D EM simulations [Figure 2.11(a), Figure 2.18, and Figure 2.23]. In addition, the peak antenna gains of the multi-feed antenna samples closely track those of the single-feed antenna samples; this demonstrates that the multi-feed antennas achieve the same radiated power as conventional single-feed antennas at boresight and verifies the on-antenna power combining.

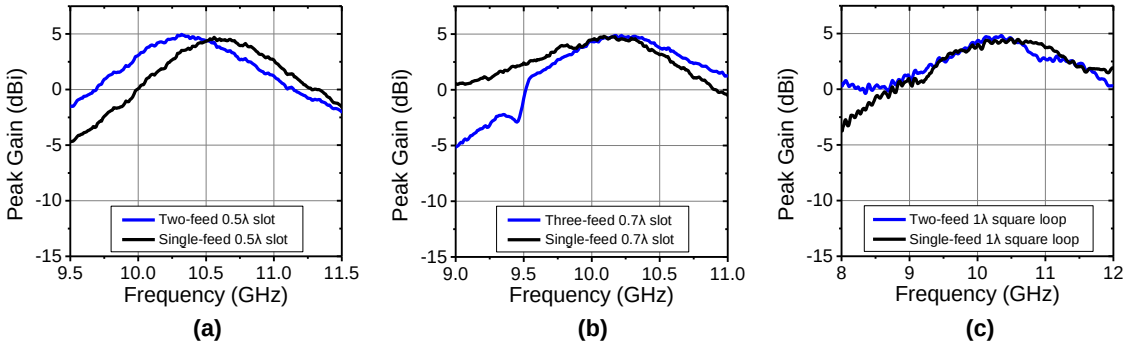

Figure 2.27 – Measured peak antenna gains for (a) two-feed and single-feed 0.5λ slot antenna, (b) three-feed and single-feed 0.7λ slot antenna, and (c) two-feed and single-feed 1λ square loop antenna.

2.5.2 Radiation Pattern Measurements

The measured far-field co-polarized radiation patterns of the 0.5λ slot antenna samples, 0.7λ slot antenna samples, and 1λ square loop antenna samples are summarized in Figure 2.28, Figure 2.29, and Figure 2.30, respectively. For the coordinates defined in Figure 2.25, the E-plane is the y-z plane, and the H-plane is the x-z plane. The measured cross-polarized radiation patterns of the 1λ square loop antenna samples are also shown in Figure 2.30. Excellent agreements between the simulation and measurement results are achieved for all the samples. More importantly, the radiation patterns of the multi-feed antennas closely match the single-feed reference antennas. This verifies that the multi-feed antennas actively synthesize the desired voltage/current distribution on the antenna and

thus indeed achieve identical radiation patterns as the conventional single-feed antennas. Moreover, together with the peak antenna gain measurement results in Figure 2.27, the multi-feed antenna has the same absolute antenna gain as the single-feed antenna in all the corresponding directions. This directly verifies the on-antenna power combining of the proposed multi-feed antenna, since the total input power is first spit by the input power divider, distributed to all the antenna feeds, and eventually combined directly on the multi-feed antenna structure for radiation. Compared with the conventional passive power combiners, the multi-feed antennas substantially increase the transmitter total radiated power with low loss and high efficiency in a very compact antenna footprint. Different from array-based spatial power combining, the multi-feed antenna achieves high-efficiency power combining without causing large array panels or reduced antenna beam-width.

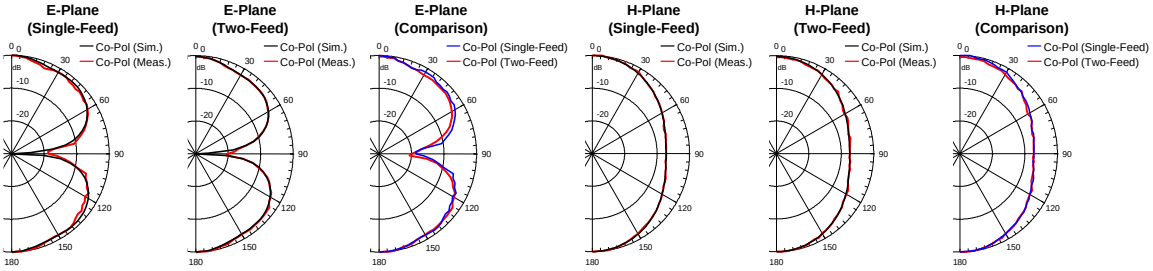

Figure 2.28 – Measured and simulated co-polarized radiation patterns of two-feed and single-feed 0.5λ slot antenna at 10.5GHz.

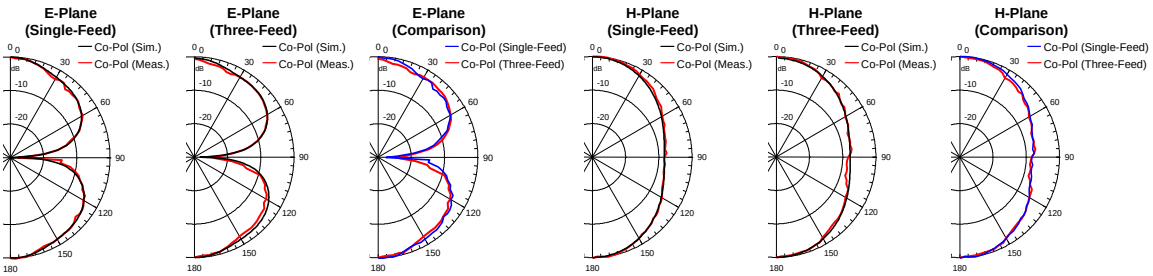

Figure 2.29 – Measured and simulated co-polarized radiation patterns of the three-feed and single-feed 0.7λ slot antenna at 10.3GHz.

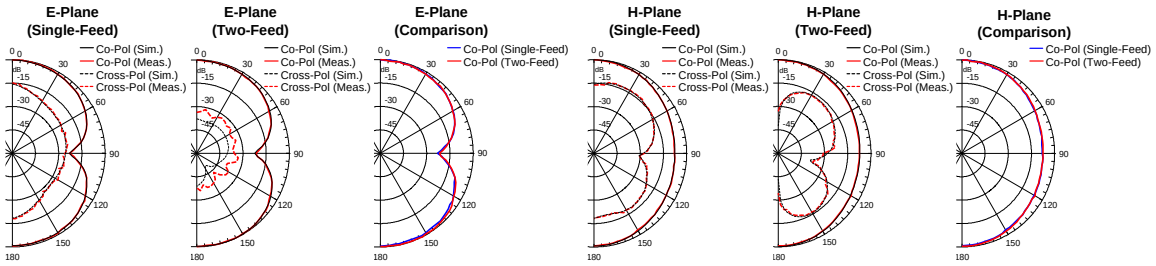

Figure 2.30 – Measured and simulated co- and cross-polarized radiation patterns of the two-feed and single-feed 1λ square loop antenna at 10.3GHz.

2.6 A 60GHz On-Chip Linear Radiator

A major challenge for low-cost silicon-based mm-wave wireless links, e.g., the 5G communication, is to provide large transmitter (Tx) output power (P_{out}) with high energy efficiency and linearity from a limited supply voltage, so that the high path loss and limited link budget at mm-wave can be compensated. To address this challenge, an on-chip linear radiator is proposed, as a multi-feed antenna driven by multiple linear PAs, which achieves very low-loss direct on-antenna power combining and boosts the total Tx P_{out} with high efficiency, demonstrating the unique advantages of circuit-antenna co-designs. Its single-element implementation in a 45nm CMOS SOI process generates +27.9dBm saturated power (P_{sat}) with 23.4% PAE and +33.1dBm peak EIRP at 59GHz [39]. It supports 4Gb/s 16-QAM signal with -21.9dB EVM and 4.8Gb/s 64-QAM signal with -25.4dB EVM [39]. The radiator element can be implemented as an array to further boost the Tx EIRP, and its frequency can be scaled to address various mm-wave applications.

The proposed radiator consists of cascaded lumped Wilkinson dividers for input power distribution, 16 unit PAs, 4-to-1 parallel power combiners at the PA outputs, and a 4-feed on-chip slot antenna for direct on-antenna power combining and radiation (Figure 2.31). The unit PA has 2 stages, comprising a Class-B cascode PA stage with 2V V_{DD} and

a Class-AB common-source driver with 1V V_{DD}. Neutralization capacitors improve the differential-mode stability and power gain. The input balun, inter-stage matching, and PA output matching network are designed using transformers for compact layout.

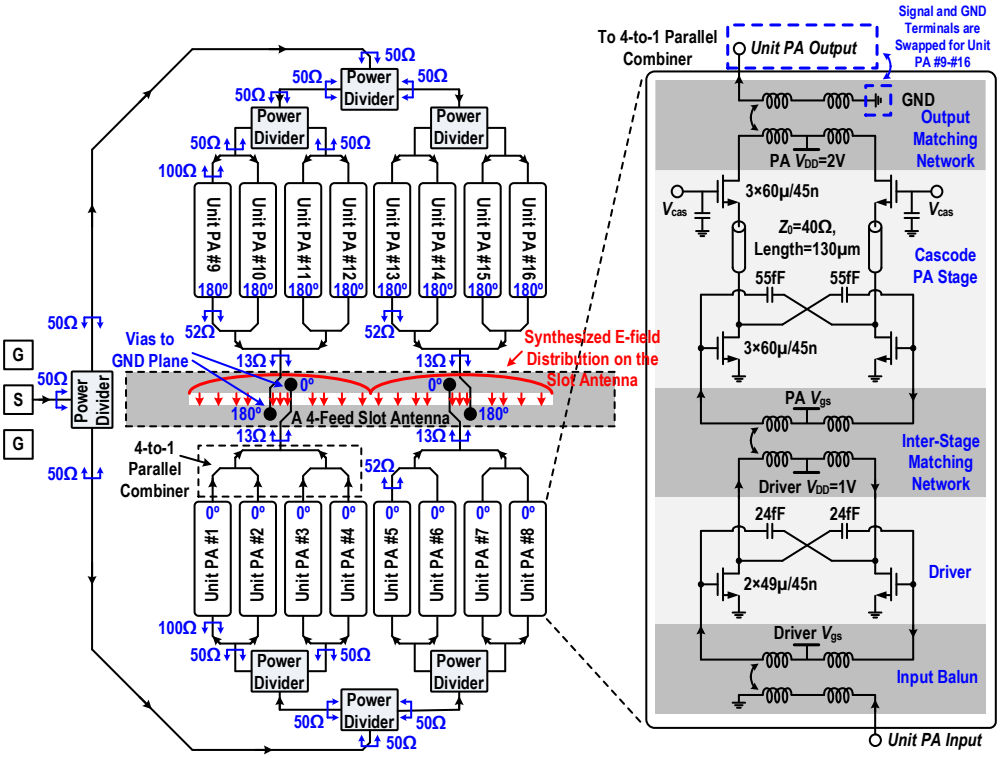

Figure 2.31 – Circuit schematic of the 60GHz on-chip linear radiator element with a multi-feed antenna implemented as a 4-feed on-chip slot antenna for direct on-antenna power combining of 16 unit 2-stage PAs.

2.6.1 60GHz On-Chip Multi-Feed Antenna

Compared with conventional single-feed antennas, the multi-feed antenna comprises multiple antenna feeds whose feeding signals collectively synthesize the desired on-antenna voltage/current profiles and then realize an identical far-field pattern as its single-feed antenna counterpart. The multi-feed antenna combines the power from multiple feeds directly on the antenna with high-efficiency. Moreover, the multi-feed antenna can

realize on-antenna power combining that down-scales the radiation impedance at each feed without extra passive network and greatly eases Tx designs.

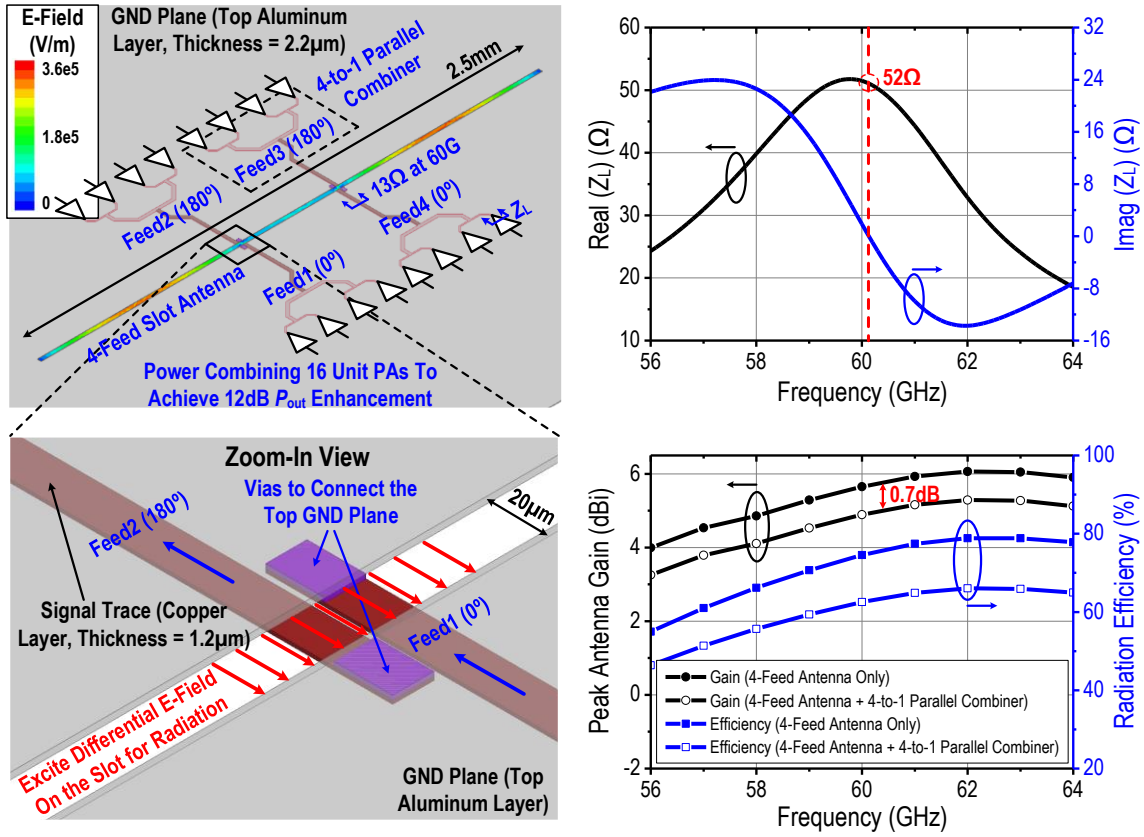

Figure 2.32 – EM-simulated synthesized E-field distribution on the 4-feed slot antenna, load impedance for the unit PA (Z_L), peak antenna gain and radiation efficiency versus frequency.

A 4-feed on-chip slot antenna and 4-to-1 parallel combiners are shown in Figure 2.32 with a zoom-in view of the feed1 and feed2. The 4 feeds are driven from two sides of the slot with equal amplitude and 180° phase difference to excite the desired differential E-field for slot radiation. The 3D EM-simulated input impedance at each feed is 13Ω at 60GHz, verifying radiation impedance down-scaling by multi-feed antenna. The 4-to-1 parallel combiner scales the feed impedance to 52Ω at each unit PA output to match the optimum load-pull impedance. The 4-feed slot antenna uses the top aluminum layer as the

ground plane and radiates from the chip backside. The high-resistivity substrate of the SOI process results in 5.6dBi simulated peak antenna gain at 60GHz, 74.5% antenna radiation efficiency, 84% (0.7dB) combiner passive efficiency, and thus 62.5% total radiation efficiency including the multi-feed antenna and combiners (Figure 2.32).

The 4-feed on-chip slot antenna and the parallel combiners combine the output power from 16 unit PAs on the antenna, achieving 11.3dB enhancement on the total output power. Note that the multi-feed antenna boosts the Tx output power in one single antenna footprint (slot size=2.5mm×20μm) without any silicon lens. Unlike array-based spatial combining, the multi-feed antenna does not enlarge the panel size or reduce the antenna beam-width.

2.6.2 Measurement Results

To evaluate the unit PA, a PA test structure (TS) is implemented in the same process (Figure 2.33). The measured TS gain is 24dB and 22.4dB at 55GHz and 60GHz, respectively. The measurement shows 16.7dBm P_{sat} and 14.6dBm P_{1dB} at 60GHz with 28.3% PAE_{max} and 22.8% PAE_{1dB}, matching well with the simulations. The PA TS P_{sat} variation is below 0.8dB from 50 to 67GHz.

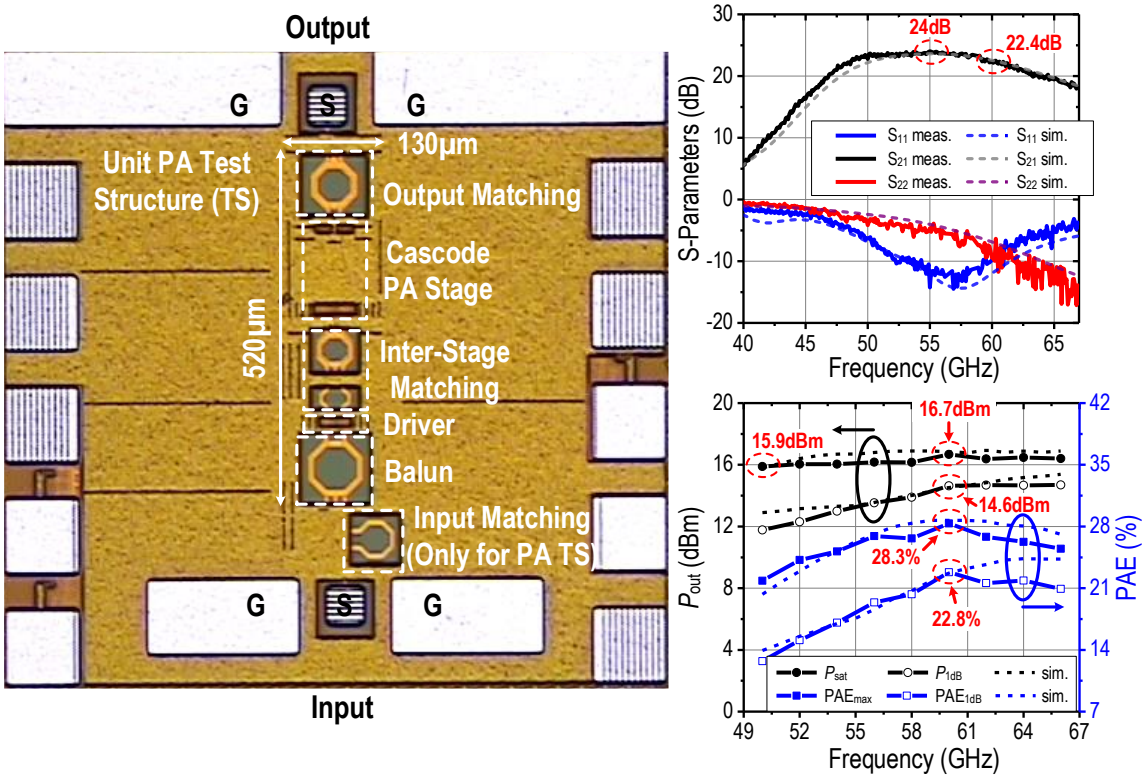

Figure 2.33 – Chip microphotograph of the unit PA test structure (TS), simulated/measured small-signal S-parameters and large-signal performance versus frequency of the TS. The additional input matching inductor is used only in the PA TS to facilitate its characterization.

Next, the radiator IC is flip-chip packaged to a Rogers CLTE-AT PCB, and the mm-wave input is fed by an end-launch connector (Figure 2.34). A horn antenna and power sensor measure the radiator's CW output at far-field (65cm). At center frequency 59GHz, the radiator achieves 33.1dBm peak EIRP (Figure 2.35). The measured E-/H-plane patterns closely match the EM simulations. The E-/H-plane ripples are due to the finite PCB ground. A full 3D scan is required to directly measure the total radiated power, which is not supported by our measurement setup. Instead, the 3D EM-simulated antenna gain is used to calculate P_{out} from measured EIRP, yielding 27.9dBm P_{sat} at 59GHz with 23.4% PAE_{max}. Alternatively, the total P_{out} is estimated using TS measurements. Considering the 12dB enhancement due to 16-PA power combining and the 0.7dB simulated parallel combiner

loss, the TS-based estimated P_{sat} is 27.8dBm, closely matching the EIRP-based P_{sat} value of 27.9dBm. The 1dB P_{sat} bandwidth is from 56.5 to 61GHz and is limited by the slot antenna. At 59GHz, the P_{1dB} is 25dBm, and the AM-PM nonlinearity measured using a sampling oscilloscope is 5.6°.

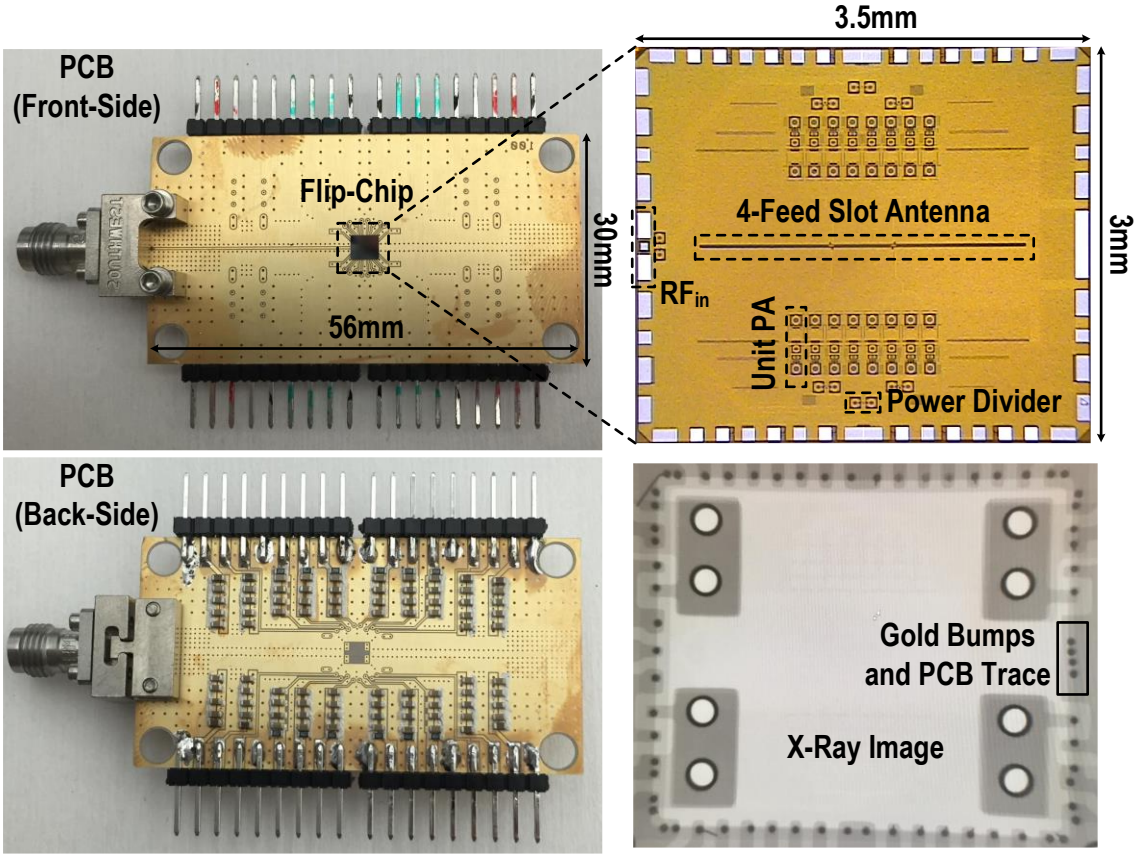

Figure 2.34 – Pictures of the flip-chip packaged PCB, chip microphotograph, and an X-ray image to verify the alignment between the flip-chip bumps and the PCB traces.

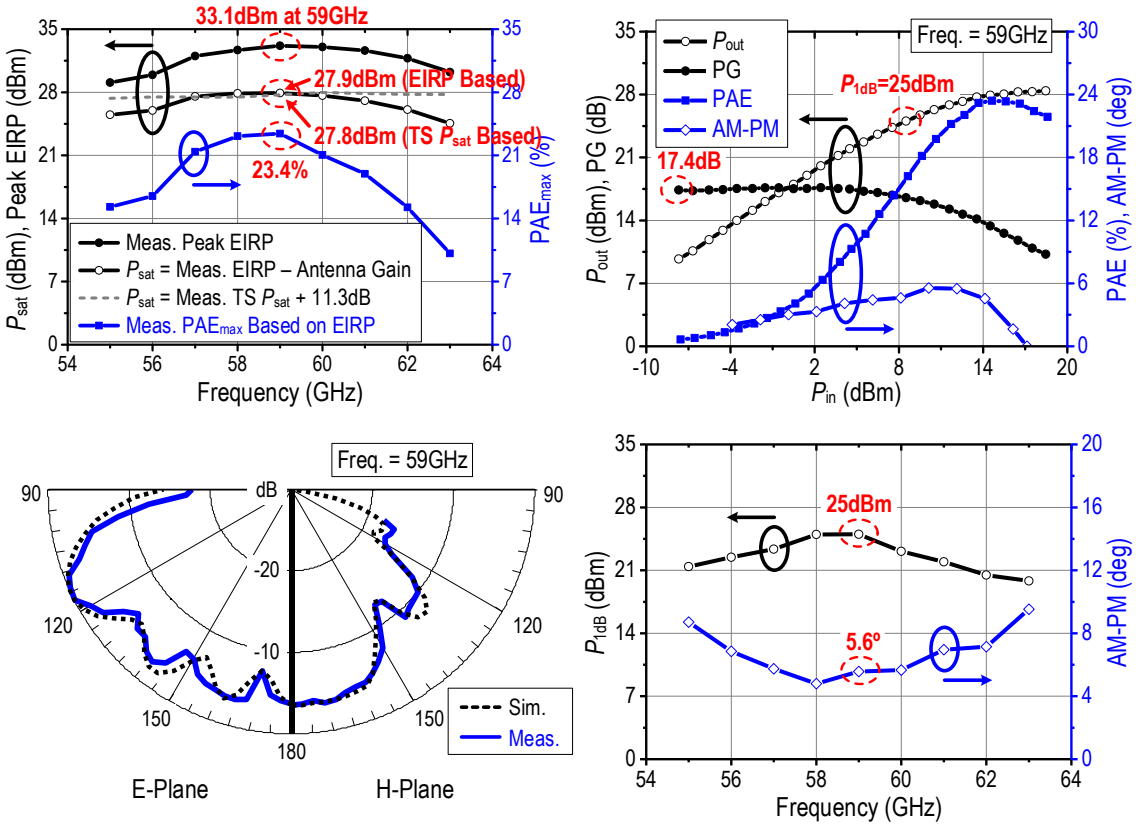

Figure 2.35 – Measured large-signal performance and radiation patterns of the linear radiator IC.

The radiator performance with complex modulations at different symbol rates is shown in Figure 2.36, Figure 2.37, and Figure 2.38. The input baseband data is generated by an AWG and is up-converted to 59GHz by an external mixer and image-rejection filter (Figure 2.39). Without any pre-distortion or channel equalization, the radiator achieves -21.9dB EVM with 20.2dBm P_{avg} for 4Gb/s (1GSym/s) 16-QAM signal, and -25.4dB EVM with 19.3dBm P_{avg} for 4.8Gb/s (0.8GSym/s) 64-QAM signal, verifying its linearity in dynamic operations. Compared with the reported 60GHz silicon PAs, this work achieves the highest P_{sat} and P_{1dB} with a very competitive PAE and data rate. The linear radiator can be scaled to an array and/or to different frequency for various mm-wave applications.

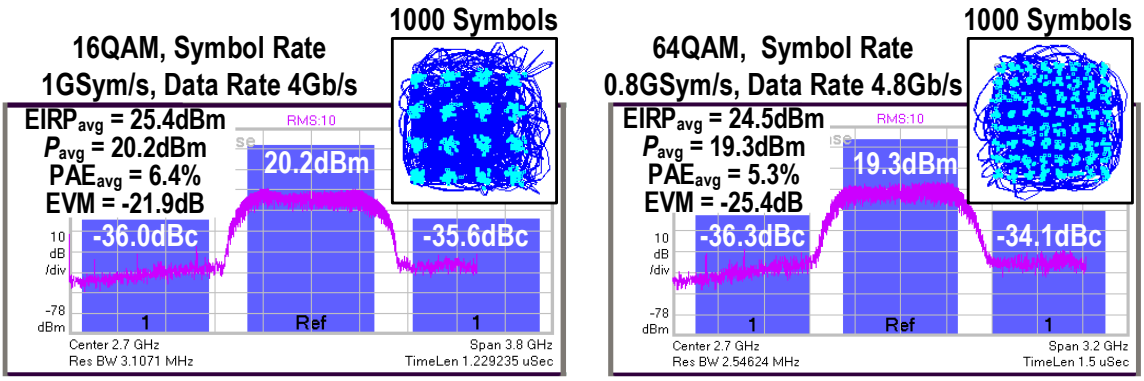

Figure 2.36 – Measured EVM and spectra for 1GSym/s 16-QAM and 0.8GSym/s 64-QAM signals at 59GHz.

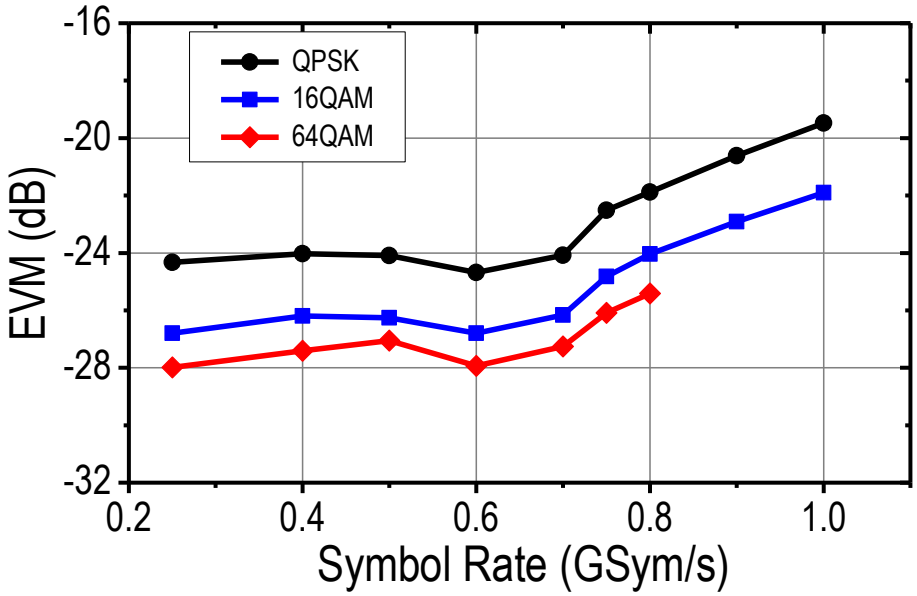

Figure 2.37 – Measured EVM versus symbol rate for QPSK, 16-QAM, and 64-QAM at 59GHz.

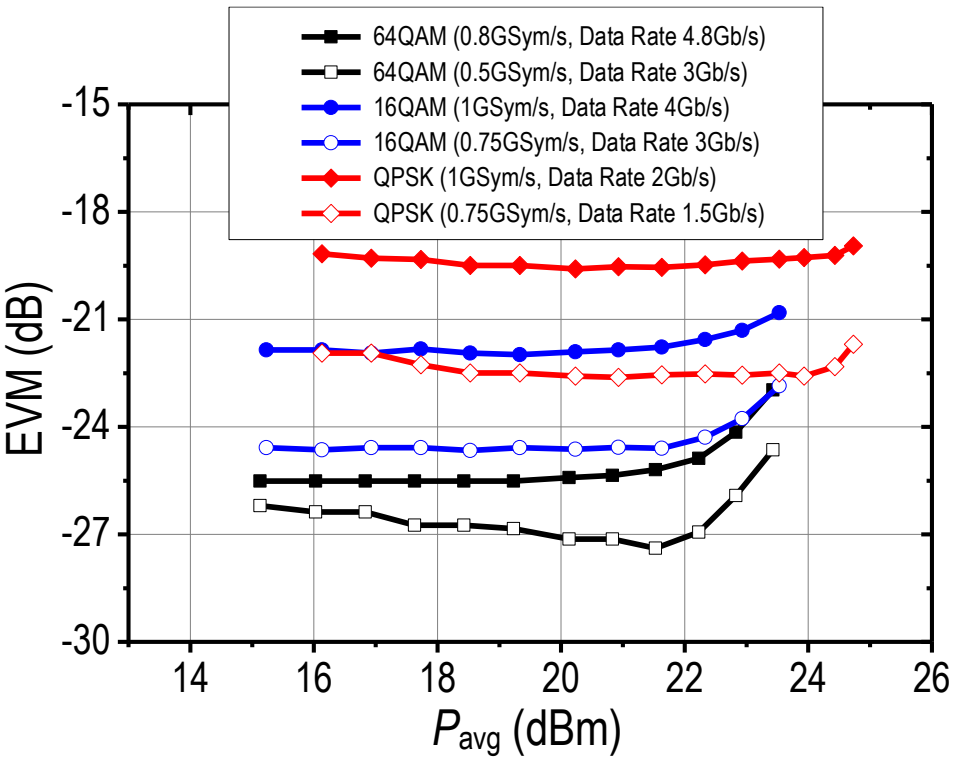

Figure 2.38 – Measured EVM of the CMOS linear radiator IC versus P_{avg} for QPSK, 16-QAM, and 64-QAM signals at 59GHz.

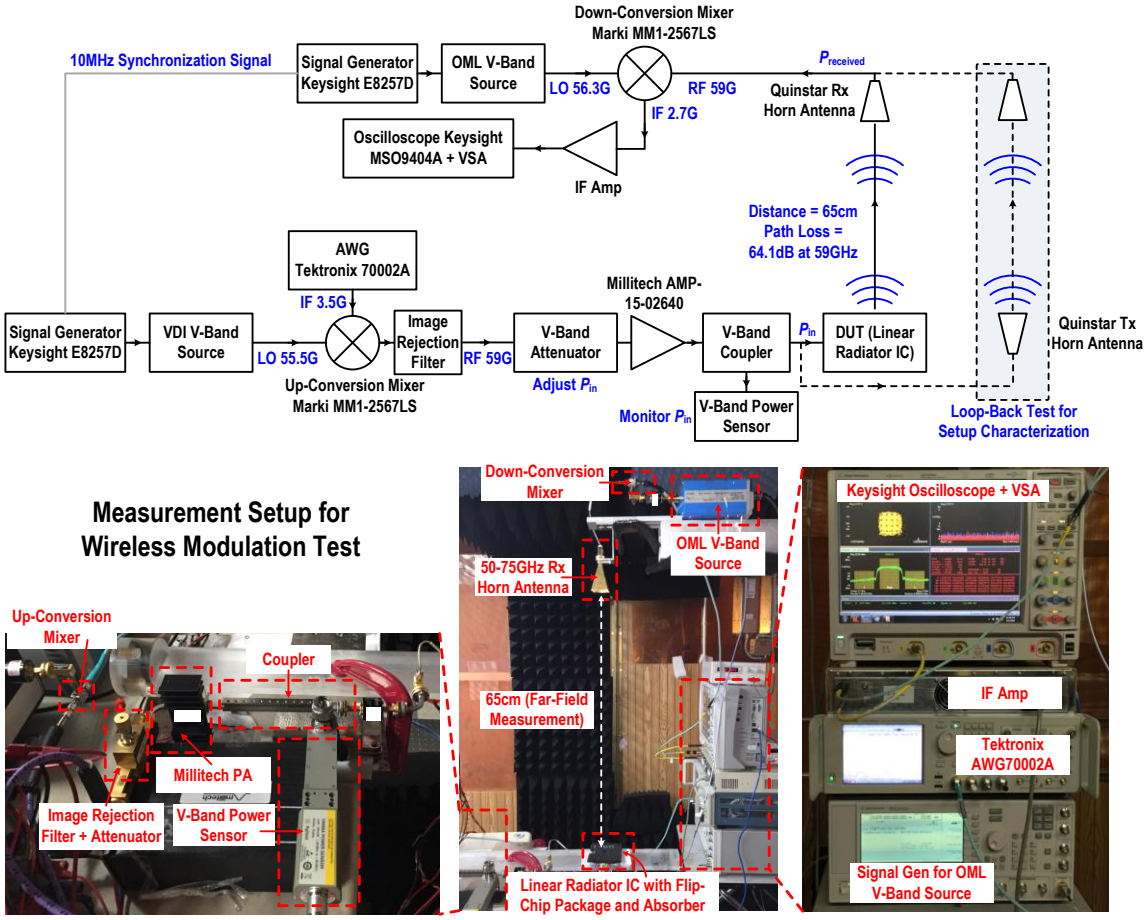

Figure 2.39 – Measurement setup for the wireless modulation test. The input data is generated by an AWG, up-converted by a mixer and then image-filtered to generate the modulated signal at 59GHz. At the far-field (65cm), the signal is received by an Rx horn antenna and then down-converted, amplified, and analyzed by an oscilloscope. In a loop-back test, a Tx horn antenna replaces the linear radiator IC to measure the EVM floor of the measurement setup.

Table 2.1 – Performance comparison with state-of-the-art mm-wave PAs in silicon.

	This Work	ISSCC 2016	JSSC 2016	ESSCIRC 2014	TMTT 2015	TMTT 2015
Frequency (GHz)	**60**	55	60	60	42.5	77
P_{sat} (dBm)	**27.9**	23.6	10.8	19.9	27.2	20.9
PAE_{max} (%)	**23.4**	27.7	29.8	20	10.7	22.3
P_{1dB} (dBm)	**25**	19.9	7.4	17.2	21**	17.8
PAE_{1dB} (%)	**16.2**	15.7	15**	10**	5**	14**
Power Gain (dB)	**17.4**	23**	24.3	32.4	18**	18.1
P_{sat} 1dB BW (GHz)	**56.5 to 61**	40 to 65	54.5 to 63.5	57 to 65**	<33 to 46	68 to 87
V_{DD}	**1V (Driver), 2V (PA)**	1.6V (Driver), 4V (PA)	0.9V	1.2V	4.8V	0.9V
Modulation Type, Data Rate, EVM, P_{avg}	**16-QAM, 2Gb/s, -26.3dB†,‡, 20.2dBm**	16-QAM, 2Gb/s, -21dB†, 14.8dBm	QPSK, 3.3Gb/s, -20.7dB†, 8.1dBm	N/A	N/A	16-QAM, 2Gb/s, -21dB†,**
	64-QAM, 3Gb/s, -27dB†,‡, 20.1dBm	64-QAM, 3Gb/s, -25dB†, 12.8dBm	16-QAM, 6.7Gb/s, -16.5dB†, 7.2dBm			64-QAM, 3Gb/s, -24.7dB†, 11.9dBm
	16-QAM, 4Gb/s, -21.9dB†,‡, 20.2dBm		QPSK, 3.3Gb/s, -23.6dB*, 5.3dBm			16-QAM, 4Gb/s, -18dB†,**
	64-QAM, 4.8Gb/s, -25.4dB†,‡, 19.3dBm		16-QAM, 6.7Gb/s, -18.1dB*, 3.6dBm			16-QAM, 4.4Gb/s, -16dB†,**
Chip Area (mm^2)	**3.5×3 (Including Pads and On-Chip Antenna)**	1.23×0.83 (Including Pads)	0.18 (Core Area)	0.7×0.45 (Core Area)	3.2×1.3 (Core Area)	0.5×0.38 (Core Area)
Topology	**16 PAs + MFA Using On-Antenna Power Combining**	Asymmetric 2-Way Combiner	Digital Polar Tx	8-Way Combiner	8-Way Combiner	Parallel-Series 4-Way Combiner
Technology	**45nm CMOS SOI**	130nm SiGe	40nm CMOS	65nm CMOS	45nm CMOS SOI	40nm CMOS

† Without Pre-Distortion ‡ Limited by the Measurement Setup

* With Pre-Distortion ** Graphically Estimated

CHAPTER 3. A MILLIMETER-WAVE FULL-DUPLEX TRANSCEIVER FRONT-END WITH AN ON-CHIP MULTI-FEED SELF-INTERFERENCE-CANCELING ANTENNA AND AN ALL-PASSIVE CANCELER

3.1 Introduction

In Chapter 2, we propose a multi-feed antenna for high-efficiency direct on-antenna power combining. The multi-feed concept can also be extended to achieve other interesting functionalities by proper driving conditions and terminations of all the antenna feeds. In this chapter, we will go one step beyond the on-antenna power combining capability, and present an on-chip multi-feed self-interference-canceling antenna for mm-wave full-duplex (FD) wireless communication [51].

Mm-wave FD transceivers (TRXs) have the potential to unlock the full throughput of future 5G links. A major challenge in mm-wave FD TRXs is to suppress the wideband modulated self-interference (SI) of the transmitter (TX) to its own receiver (RX) with ~100dB cancellation over a large instantaneous bandwidth. This often requires distributed cancellations across the antenna, RF, and digital domains [52].

The antenna-domain self-interference cancellation (SIC) is critical since it directly relaxes the RX linearity requirement [52]. Practical antenna SIC solutions should provide low loss, compact footprint, and a large modulation bandwidth. Several antenna-interface SIC techniques are demonstrated in silicon, each with advantages/limitations for wideband high mm-wave applications. First, reciprocal electrical-balance duplexers [53] suffer from

3dB signal loss, directly degrading TX output power (P_{out})/efficiency and RX noise figure (NF). Second, non-reciprocal circulators [54] are also lossy (~3dB) and require large LO driving power, which is challenging for high mm-wave bands. Finally, a 60GHz TX/RX antenna pair with an auxiliary reflective termination is reported; it requires frequency-dependent tuning and introduces 0.5-1dB additional loss for both TX/RX paths [52]. Dual TX/RX antennas also occupy a large area and are undesirable for massive MIMOs.

The RF-domain SIC is equally important to further suppress the SI and relax the downstream RX, e.g., ADC, dynamic range. For future FD massive MIMOs, desirable RF SIC solutions should offer ultra-low power, large dynamic range, orthogonal amplitude/phase tuning, and large instantaneous bandwidth.

In this chapter, we propose a multi-feed SIC antenna that provides a high TX-RX isolation (>35dB in measurement), an instantaneous broad bandwidth (60-75GHz), and no additional TX/RX-path signal loss, in only one antenna footprint. An all-passive zero-power RF canceler is integrated with nearly orthogonal amplitude/phase tunability to further enhance SIC. As a proof of concept, 2 FD TRX front-end chips are used to establish a 4Gb/s FD wireless link before using any digital SIC [51].

3.2 On-Chip Multi-Feed Self-Interference-Canceling Antenna

The proposed FD TRX front-end consists of an on-chip 4-feed SIC slot-loop antenna, 2 parallel TX paths, 2 parallel RX paths, and a passive canceler (Figure 3.1). The 4-feed antenna supports 2 concurrent radiation modes with orthogonal polarizations, one for TX and one for RX. For the TX, 2 TX feeds are driven differentially, synthesizing a standing-wave voltage distribution on the slot loop. Due to the symmetry, the TX signals

have 2 voltage nulls at the 2 RX input feeds, naturally providing high TX/RX antenna isolation. The 2 TXs are directly power-combined on the antenna for low-loss high-efficiency radiation, while the 2 RX feeds enable low-loss on-antenna power splitting to extend RX linearity and ensure its sensitivity. More importantly, the proposed antenna SIC relies on its symmetry and is inherently frequency independent, yielding an instantaneous broadband SIC with no frequency-tuning element.

Phase shifters (PS) and variable gain amplifiers (VGA) are integrated in the 2 sub-TXs to compensate their potential mismatch. Leveraging the SOI process high-resistivity substrate, the EM-simulated 4-feed antenna radiation efficiency is 91.2% at 70GHz with the 2 RX feeds loaded, even assuming 1dB amplitude and 10° phase mismatches between the 2 sub-TXs. This radiation efficiency closely matches that of a 2-feed antenna with only 2 TX feeds. Therefore, compared to the dual TX/RX antennas [52], the multi-feed SIC antenna enables FD TX/RX operation in only one antenna footprint but without major loss penalty on TX P_{out} and RX NF.

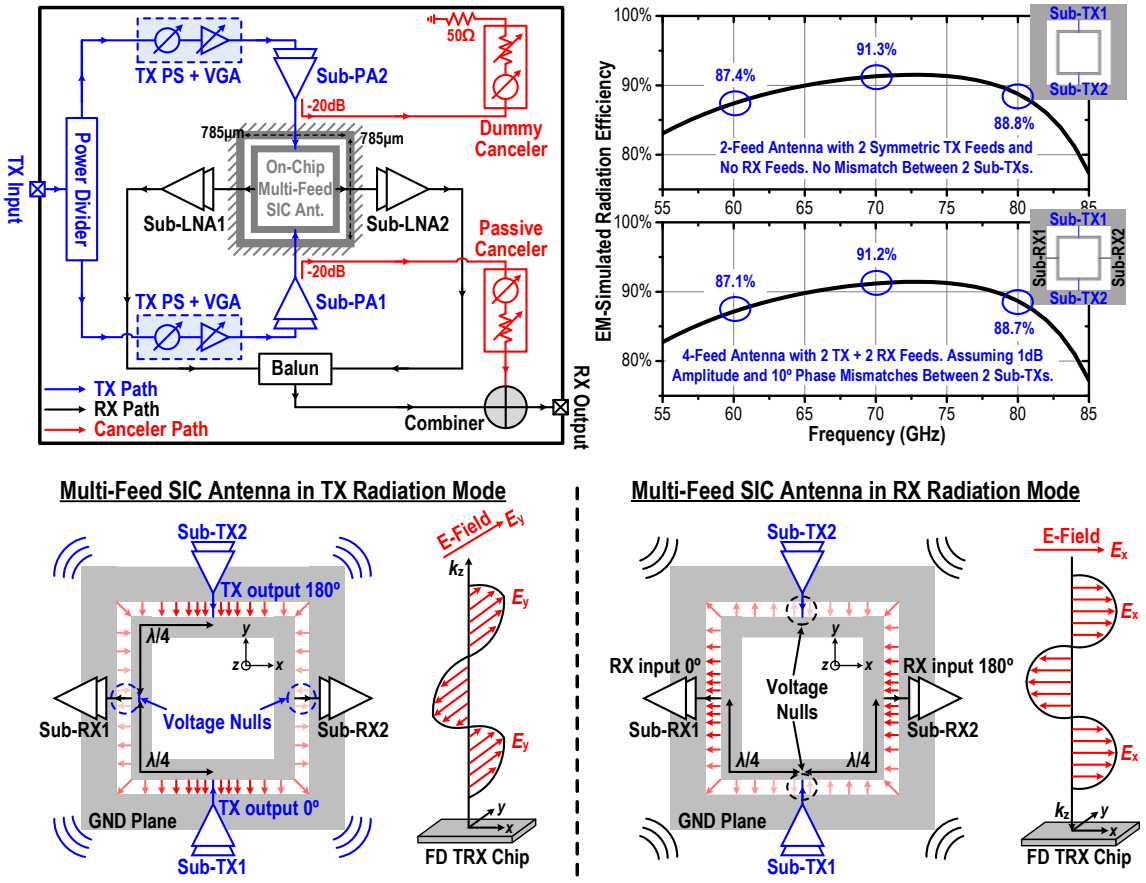

Figure 3.1 – System architecture of the mm-wave full-duplex transceiver front-end, EM-simulated antenna radiation efficiency, and full-duplex operation principles of the on-chip multi-feed SIC antenna (785μm×785μm).

3.3 All-Passive RF Canceler

The all-passive RF canceler is shown in Figure 3.2. Its zero DC power consumption and large linearity are particularly suitable for massive MIMOs, where each RX element needs multiple cancelers to suppress its self-/neighbor-interferences. A small TX replica feeds the RF canceler via a -20dB capacitive coupler, and is amplitude-scaled by cascaded reflection-type attenuators (RTA) and phase-shifted by reflection-type phase shifters (RTPS). Then, the cancellation signal is combined with the RX balun output by a Wilkinson combiner. Both RTA and RTPS use wideband compact transformer-based 90°

couplers (Figure 3.2). RTA is inherently phase-invariant during amplitude tuning, and it offers 0°/180° phase shift when the tunable NMOS resistors are set above/below the coupler characteristic impedance (50Ω). The simulated RF canceler total attenuation and its total phase shift at 70GHz is shown in Figure 3.2. Since the last-stage RTA adds 0°/180° phase shift, the required RTPS continuous phase tuning is reduced from 360° to 180°, enabling low loss variation (<3dB) during its phase shifting. Thus, the all-passive canceler supports nearly orthogonal and continuous amplitude/phase tuning, greatly easing the canceler adjustment.

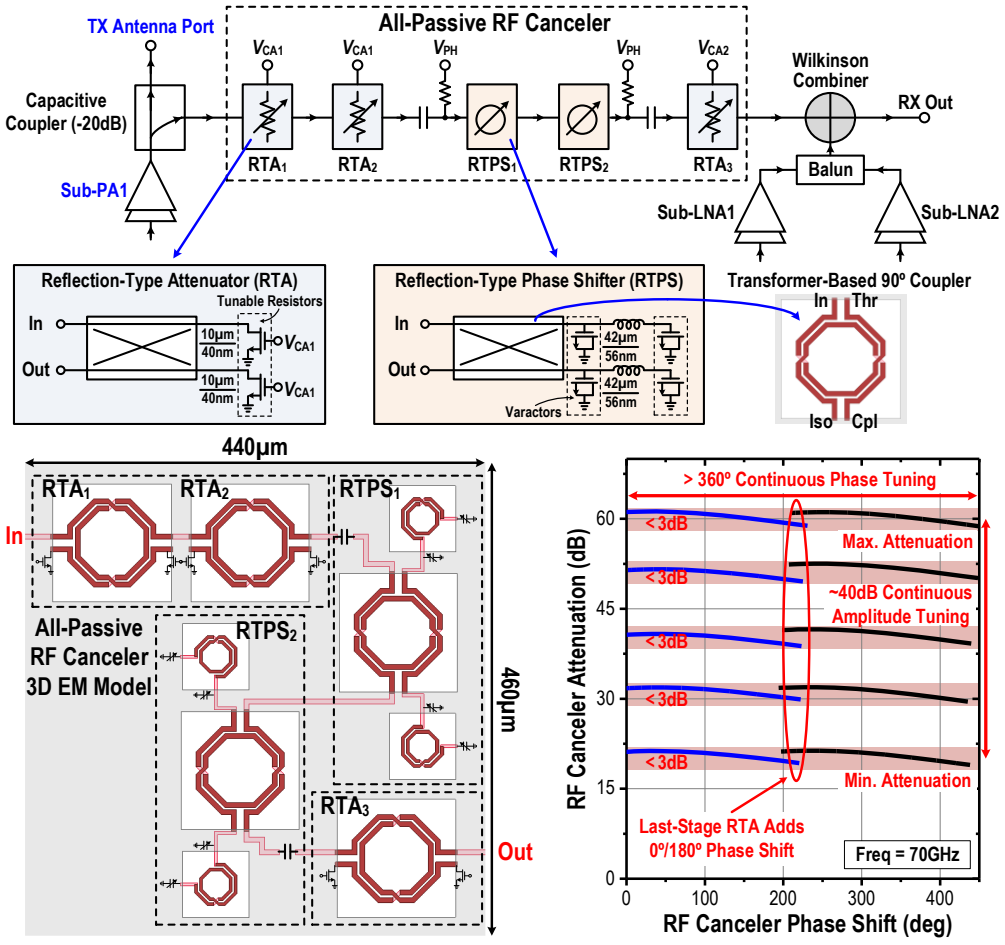

Figure 3.2 – Schematic and 3D EM model of the all-passive RF canceler, and simulated RF canceler total continuous attenuation and its total continuous phase shift at 70GHz, showing nearly orthogonal amplitude/phase tuning.

3.4 TX and RX Building Blocks

To support Gb/s wireless communication with a sufficient link budget, large TX P_{out} and high efficiency are essential. In the TX, each sub-PA contains one common-source driver and one cascode output stage both with neutralization (Figure 3.3). The differential sub-TX output signals at the 2 TX antenna feeds are generated by exchanging the signal/ground terminals of the PA output transformers, which are co-designed with the on-chip antenna for broadband matching (Figure 3.3). The TX PS is a varactor-loaded transmission line, providing a simulated 20° phase tuning range with <0.5dB loss variation at 70GHz. The VGA is a one-stage cascode amplifier with a PMOS tunable load. An extra 400Ω load reduces the output quality factor and minimizes VGA phase variation over gain settings. The simulated gain tuning range is 1-6dB with <3° phase variation. The small PS loss variation and small VGA phase variation also enable nearly orthogonal amplitude/phase tuning and fast sub-TX mismatch calibrations. In the RX, the LNA has 2 cascode stages with input inductive degeneration, and the 2 sub-RX outputs are combined by a broadband balun.

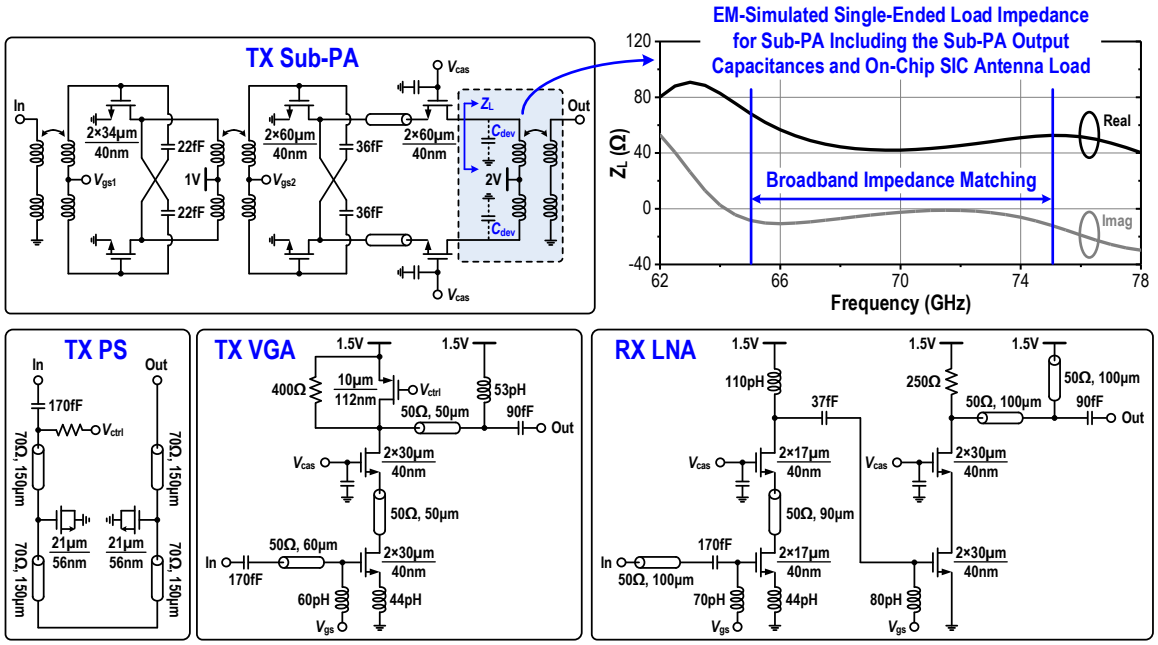

Figure 3.3 – Schematic of the sub-PA, TX PS, TX VGA, RX LNA, and simulated sub-PA load impedance (Z_L) including the sub-PA output capacitances and on-chip SIC antenna load.

3.5 Measurement Results

The FD TRX front-end is implemented in a 45nm CMOS SOI process. The chip micrographs are shown in Figure 3.4. The individual TX/RX performance is measured first (Figure 3.5). In the TX continuous-wave (CW) tests, a horn antenna and a power sensor measure the TX EIRP at the far-field. The 3D EM-simulated antenna gain is used to calculate TX P_{out} from measured EIRP. At 64GHz, the TX achieves 18.5dBm P_{sat}, 16.5dBm P_{1dB}, 23.5% PAE_{max} and 19.4% PAE_{1dB}, demonstrating high efficiency and linearity. The P_{sat} 1dB bandwidth is 62-71GHz. The TX also supports high-quality 1Gsym/s (6Gb/s) 64-QAM wireless transmission with no digital pre-distortion (DPD). In the RX individual testings, a far-field horn antenna transmits a CW signal to the FD TRX chip. The RX output is amplified by an external LNA, down-converted, and monitored by a spectrum analyzer. The RX measures a 10.9dB gain and 4.8dB minimum NF.

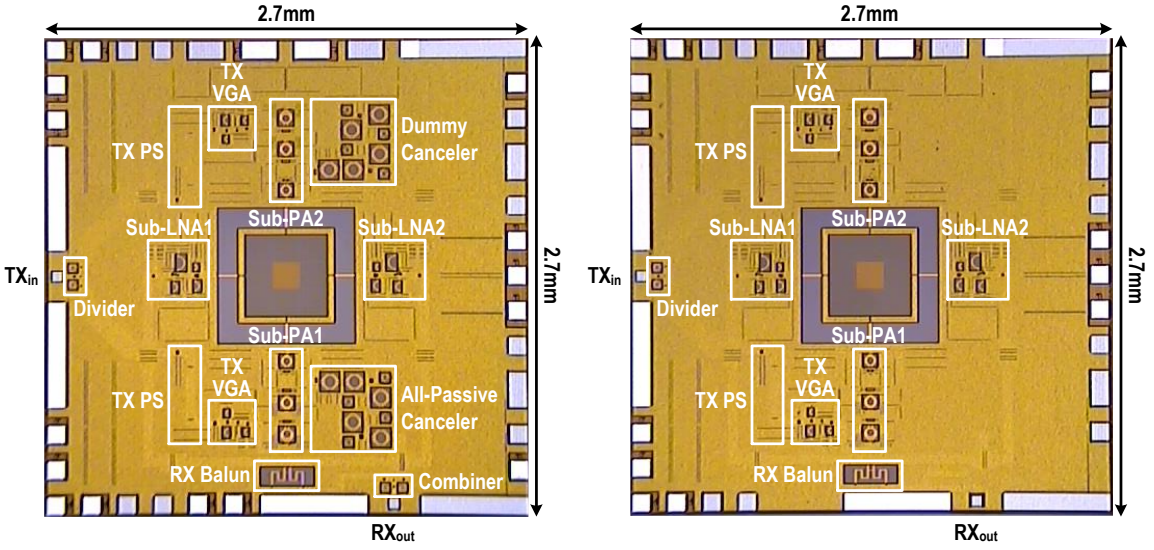

Figure 3.4 – Chip micrographs of the FD TRX front-end with RF canceler (left) and without RF canceler (right).

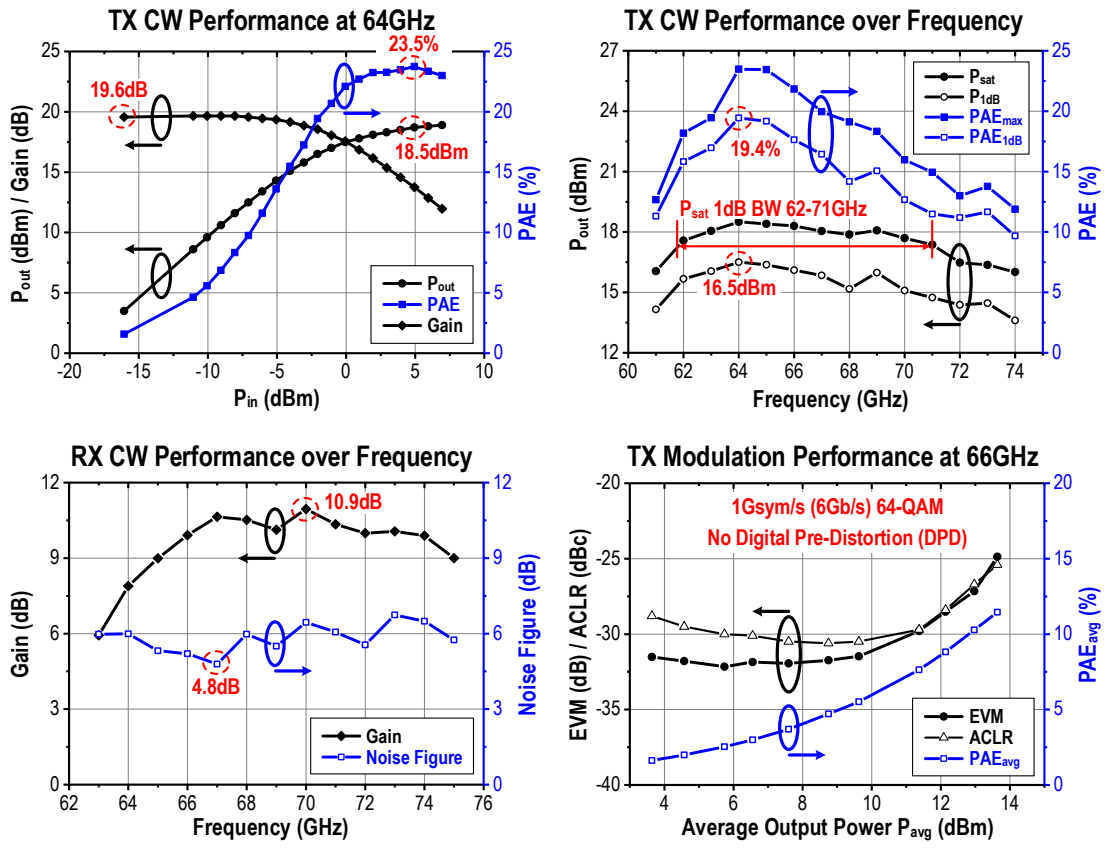

Figure 3.5 – Measured individual TX and RX continuous-wave (CW) performance, and measured EVM, ACLR, and PAE_{avg} versus average output power P_{avg} for 1Gsym/s (6Gb/s) 64-QAM signal in the TX radiation mode.

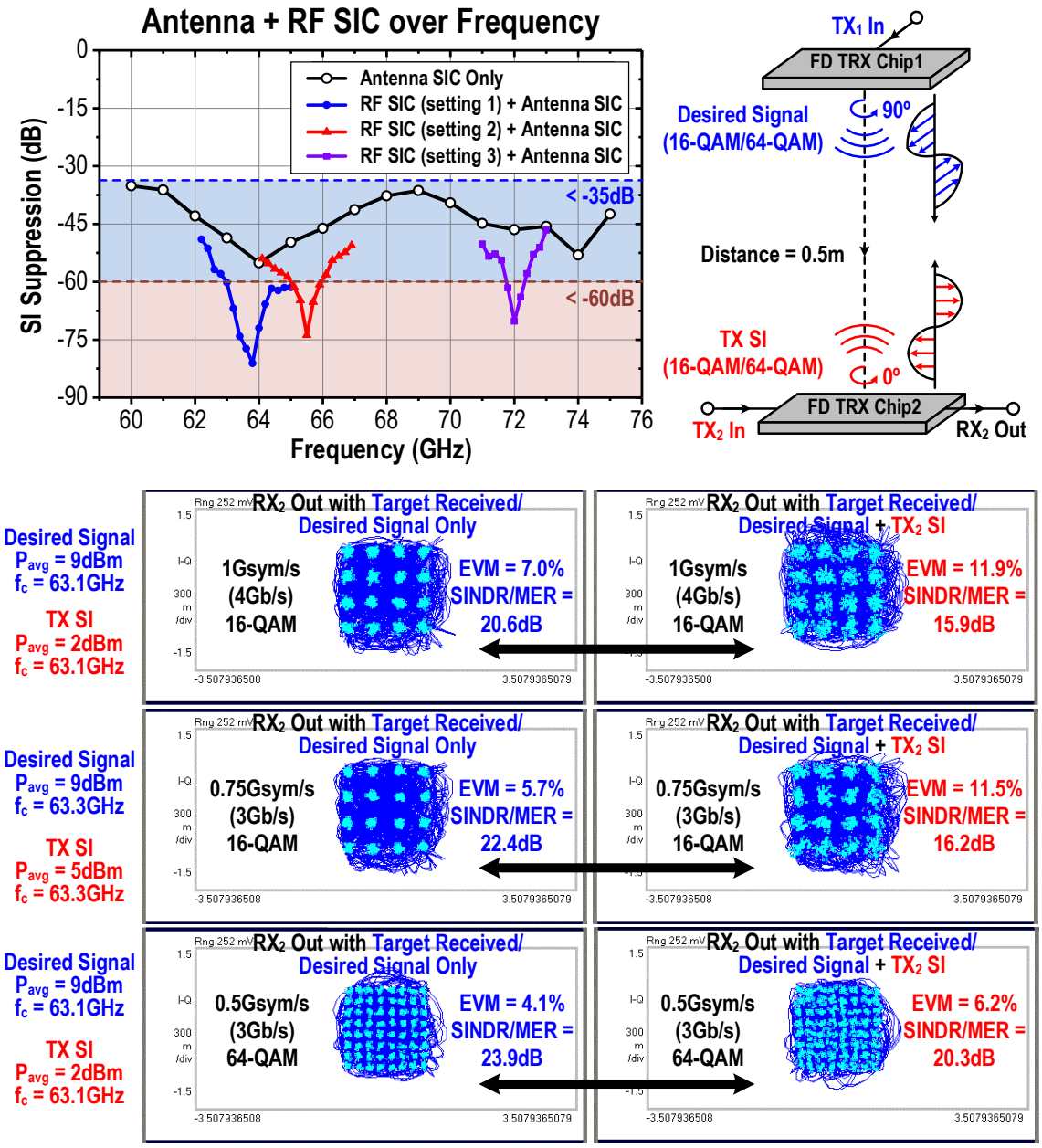

Figure 3.6 – Measured antenna SIC and total SIC over carrier frequency with different canceler settings. A direct chip-to-chip FD link is demonstrated over 0.5m between two FD TRX chips with 16-QAM/64-QAM as the target receiving/desired signal, while the TX SI uses the same modulation scheme and rate at the same carrier frequency but with independent PRBS data.

Next, both TX and RX are turned on to measure the SIC over frequency using CW signal (Figure 3.6). An FD TRX chip without RF canceler is used to test the individual antenna SIC, showing measured antenna SIC >35dB at 60-75GHz. Then, an FD TRX chip

with RF canceler is measured. Under 3 different canceler settings, the total antenna+RF SIC is >60dB at 63-65GHz, 65-66GHz, and 71.7-72.3GHz, supporting reconfigurable and instantaneous wideband SIC.

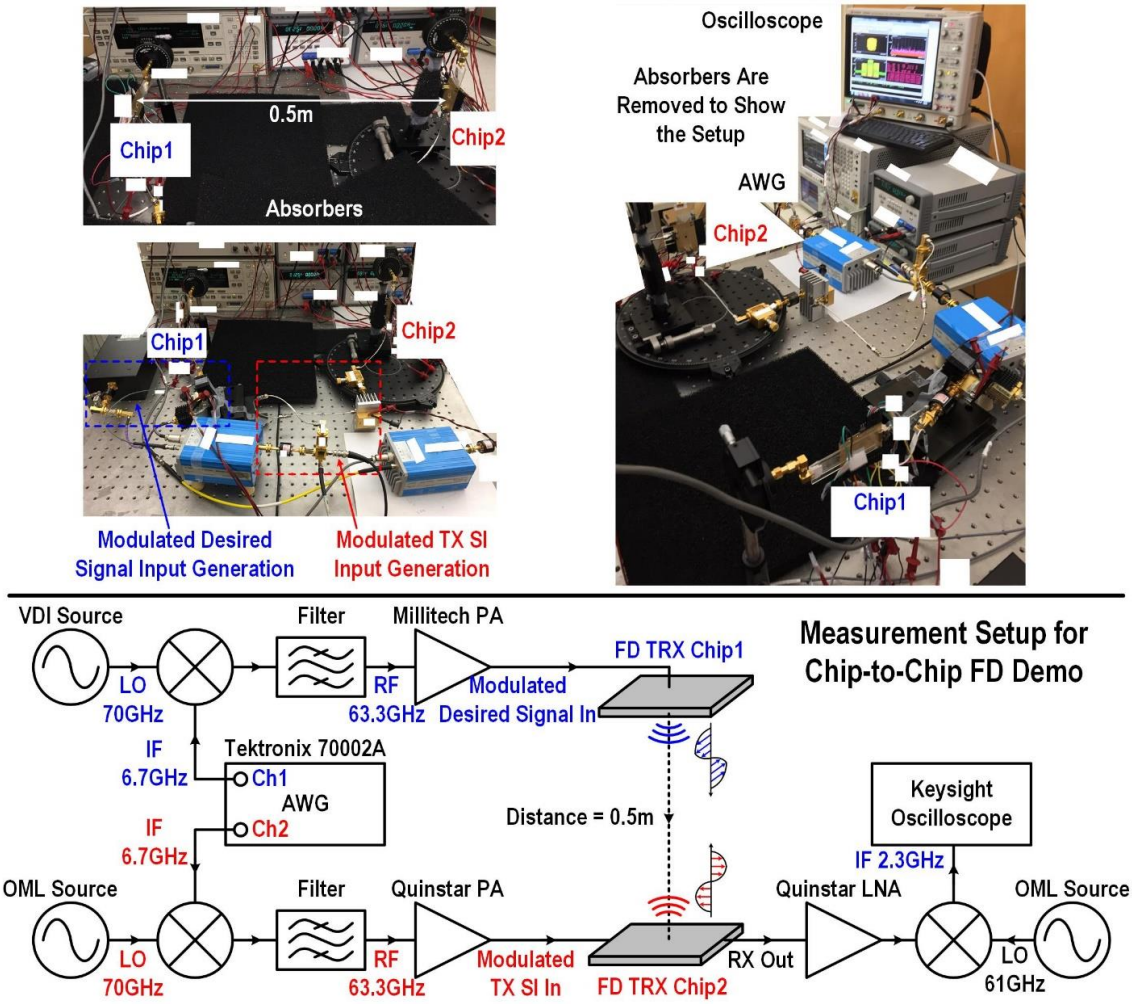

Figure 3.7 – Measurement setup for the FD demonstration over 0.5m between 2 FD TRX front-end chips. Chip1 transmits the desired modulated signal, while Chip2 simultaneously transmits another independent signal with the same modulation scheme/rate at the same carrier frequency. Two independent baseband signals are generated by two channels of an AWG, up-converted, filtered, amplified, and the RX output is down-converted and demodulated by an oscilloscope. No digital SIC or digital pre-distortion is used in these measurements.

Table 3.1 – Performance comparison with state-of-the-art mm-wave FD TRX.

		This Work				JSSC 16
Implementation	Antenna-Domain SIC Architecture	**Multi-Port SIC Antenna in One Antenna Footprint**				Dual TX/RX Antennas with An Auxiliary Reflective Term.
	Technology	**45nm CMOS SOI**				45nm CMOS SOI
	Size	**2.7mm×2.7mm (TRX Front-End + On-Chip Antenna)**				1.3mm×3.4mm (TRX Chip)
						2.4mm×3.4mm* (PCB Ant.)
TRX Metrics	Frequency Range	**60-75GHz**				57-66GHz
	TX P_{sat}, Peak PAE	**18.5dBm, 23.5%**				14.3dBm†, 18.9%†
	TX P_{1dB}	**16.5dBm**				N/A
	RX Minimum NF	**4.8dB**				4.52dB†
FD Metrics	Antenna SIC	**>35dB (60-75GHz)**				N/A
	Antenna + RF SIC	**>60dB (reconfigurable, 63-65GHz, 65-66GHz, 71.7-72.3GHz, etc.)**				>65dB (58.5-59.5GHz)
	Additional TX/RX Loss Due to Antenna SIC	**~0 (sim.) / ~0 (sim.)**				1.1dB (sim.) / 0.52dB (sim.)
	Canceler DC Power	**0**				44mW
FD Demonstration	Link Distance	**0.5m****			**0.8m****	0.7m
	Wireless Link Setup	**FD Chip to FD Chip**			**Horn Ant. to FD Chip**	Horn Ant. to FD Chip
	Carrier Frequency	**63.1GHz**	**63.1GHz**	**63.3GHz**	**63.5GHz**	59.3GHz
	Target Receiving Signal	**4Gb/s 16-QAM**	**3Gb/s 64-QAM**	**3Gb/s 16-QAM**	**3Gb/s 64-QAM**	Single-Tone Continuous-Wave
	TX SI	**4Gb/s 16-QAM**	**3Gb/s 64-QAM**	**3Gb/s 16-QAM**	**3Gb/s 64-QAM**	1Gb/s BPSK
	Desired Signal and TX SI $EIRP_{avg}$ Difference	**7dB****	**7dB****	**4dB****	**3dB****	4.7dB
	RX Output	**15.9dB SINDR/ MER**	**20.3dB SINDR/ MER**	**16.2dB SINDR/ MER**	**19.8dB SINDR/ MER**	7.2dB SINDR
	Off-Chip Digital SIC	**No**	**No**	**No**	**No**	Yes

* Graphically estimated

** Adding digital SIC (typically with ~20dB SIC) will further extend the FD link distance. If a fully symmetric FD link is needed, this will also be enabled by adding the digital SIC schemes that will equalize the EIRP difference between the target receiving signal (desired signal) and the self-TX transmission signal (TX SI).

† Include the simulated signal loss due to the auxiliary reflective termination on the dual TX/RX antennas

Finally, an FD link is demonstrated over 0.5m between 2 FD TRX chips (Figure 3.6). The measurement setup is shown in Figure 3.7. In the FD wireless link demonstration, chip1 transmits the desired modulated signal, while Chip2 simultaneously transmits an independent signal as TX SI with the same modulation scheme/rate at the same frequency. The demodulated Chip2 RX outputs demonstrate successful FD communication using 4Gb/s 16-QAM and 3Gb/s 64-QAM with no digital SIC or DPD. If a symmetric Gb/s mm-

wave FD link is needed, digital SIC (typically with ~20dB SIC [52]) can be added to readily equalize the two chips' EIRP. To the best of the authors' knowledge, this is the first mm-wave FD link that supports Gb/s modulated signals simultaneously through the TX and RX before any digital SIC. A performance summary and comparison with state-of-the-art mm-wave FD TRX is shown in Table 3.1.

CHAPTER 4. A BIDIRECTIONAL TERAHERTZ PICO-RADIO IN CMOS FOR WIRELESS SENSOR NETWORKS AND INTERNET OF THINGS

A CMOS bidirectional low-power Terahertz (THz) pico-radio with 0.57mm^2 chip area is presented in this chapter. The THz operation (320GHz) and bidirectional transmitter/receiver (TX/RX) circuit sharing architecture enable radio ultra-miniaturization for field-deployable sensors and Internet-of-Things (IoT) applications. In the TX mode, the THz pico-radio is configured as a harmonic oscillator that is modulated by digital OOK or M-ary ASK data for direct bits-to-THz transmitting. In the RX mode, the THz pico-radio is configured as a super-harmonic super-regenerative RX for direct THz-to-bits receiving with high sensitivity and low power, and an on-chip time-to-digital converter (TDC) with 25ps timing resolution measures the RX oscillation start-up time. An on-chip two-feed slot antenna is shared by the TX/RX for THz radiation and receiving without using any silicon lens. A wireless communication link between two THz pico-radio chips is demonstrated. The THz pico-radio achieves power-performance scalable operation that can be optimally set according to the actual link distance and required data rate. It supports 4.4Mb/s OOK communication over 50cm at 49.3mW peak DC power and 1Mb/s OOK communication over 17cm at 18.7mW peak DC power with BER<10^{-7}. It also supports 4-bit 16-ary ASK communication over 17cm at 57.2mW peak DC power with BER<10^{-5}.

4.1 Introduction

Highly miniaturized, low-power, and low-cost radio platforms serve as the technology foundation for various field-deployable and large-scale sensor applications, including wireless sensor networks, medical implants, and Internet-of-Things (IoT) links. Several existing low-power standards, such as Bluetooth Low Energy [55]–[58], ZigBee [59]–[61], and WBAN (IEEE 802.15.6) [62]–[64], have been proposed for wireless sensor networks and IoT applications, all of which are based on MHz–GHz radio solutions. For the state-of-the-art GHz low- power radios, the peak DC power has been reduced to several milliwatts or below with Mb/s data rate [65]–[70], sufficient for many short-range IoT applications. However, one of the governing factors for the physical sizes of MHz–GHz low-power radios is the antennas, which are often at millimeter to centimeter scales, far larger than the radio electronics. This sets a fundamental limit on the ultimate radio size scaling. As a result, these MHz–GHz radio platforms only offer radio form-factor above $10mm^3$ ($10^{-8}m^3$). Leveraging the mm-wave frequency for size-reduced low-power radio is reported in [71], and it still occupies $4.4mm^2$ chip area and $0.53mm^3$ ($5.3\times10^{-10}m^3$) radio volume including the on-chip antennas with the chip thickness of 120μm.

Recently, there is an increasing need for radical radio node miniaturization to enable emerging distributed sensing, tagging and communication applications in defense and commercial spaces that are based on densely deployed, collaborative, and secured sensor networks. These applications include very-large-scale real-time position and motion tracking, temperature and humidity monitoring, vibration and deformation sensing, as well as non-contact meter-range electromagnetic “tactile sensing” [72]–[74]. If the whole radio can be pushed to the sub-millimeter scales, the deployed radio nodes will become close to

invisible in practice, thus enhancing the security and easing the deployment. These sub-millimeter-scaled radios also enable orders-of-magnitude increase in the number of radios deployed. Together with energy harvesting/storage devices [75]–[77] and *in-situ* low-power feature-extraction computation [78]–[80], these densely deployed "invisible" short-range radios can form self-organized and autonomous networks that support meter-scale direct neighbor-to-neighbor links and long-distance information relay to gate-way terminals, e.g., UAVs, UGVs, or mobile base stations (Figure 4.1).

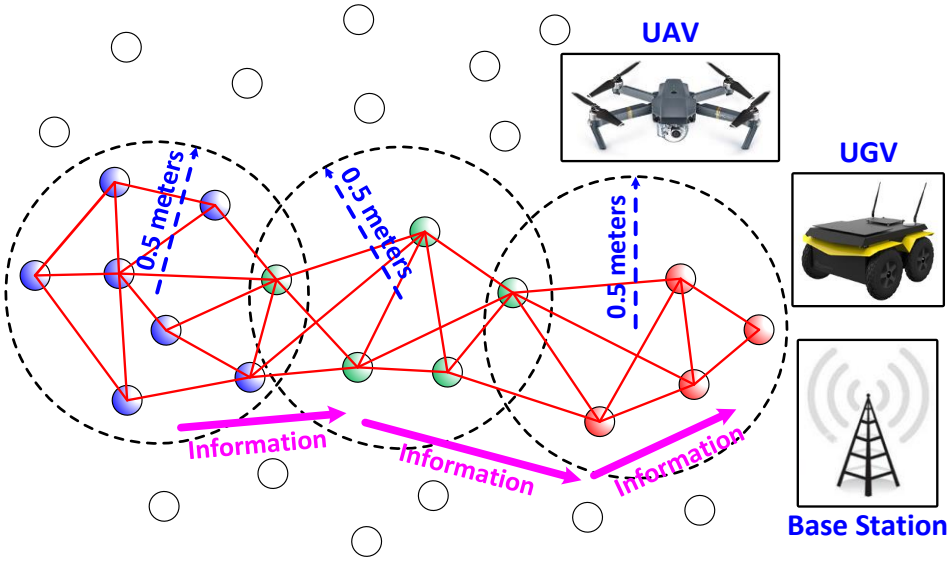

Figure 4.1 – A mesh network structure that connects massively deployed short-range (~0.5m) THz pico-radio nodes and allows them to relay the sensing information from each node to the gate-way terminals over a long distance.

The continuous device scaling in silicon IC technologies has opened the door to low-cost silicon-based electronics and radios operating at Terahertz (THz) frequencies [81]–[87]. Using THz carriers allows for a drastic antenna size reduction and enables extreme miniaturization of the whole radio to sub-millimeter scale to support future invisible sensor nodes. Moreover, employing sub-mm-wave spectrum also enables unique sensing capabilities, such as sensitive humidity monitoring and THz electromagnetic

"tactile sensing". Nevertheless, most existing THz radios require substantial DC power, often from hundreds of milliwatts to Watts, incompatible with field-deployable radio nodes. Moreover, THz communication systems typically exhibit challenges in high path loss, signal generation, and high-sensitivity signal receiving.

Therefore, the motivation of this work is to present the first exploratory study for designing IoT devices using THz frequencies to achieve a sub-millimeter-scale form factor. A digital-bits-in/-out CMOS low-power 320GHz pico-radio is implemented and characterized. It demonstrates the feasibility of using low-power THz electronics to form a short-range high-quality wireless link with sufficient data-rate, while naturally enabling radio ultra-miniaturization for future massively deployed invisible sensor networks [40]. As a proof-of-concept link demonstration, two of our developed THz pico-radio chips are used to establish a wireless link with up-to 4.4Mb/s On-Off Keying (OOK) modulation and 16Mb/s 4-bit 16-ary Amplitude-Shift Keying (ASK) modulation in a TDD (time division duplex) manner. A bidirectional transmitter/receiver (TX/RX) circuit-sharing architecture configures the radio as a harmonic oscillator in the TX mode or as a super-harmonic super-regenerative receiver (SRR) in the RX mode. The TX and RX modes both utilize nonlinear and oscillatory (regenerative) operations of the active devices, enabling the low-power radio communication at THz. With the TDD operation, an on-chip two-feed slot antenna is shared by the TX/RX to eliminate any duplexer for further radio size reduction [12]. The chip area is only 0.57mm^2 including the on-chip antenna.

This chapter is organized as follows. Section 4.2 presents the design details of the proposed bidirectional THz pico-radio. The experimental results are shown in Section 4.3. Section 4.4 concludes this chapter with a performance comparison table.

4.2 Bidirectional THz Pico-Radio Implementation

4.2.1 TX Mode

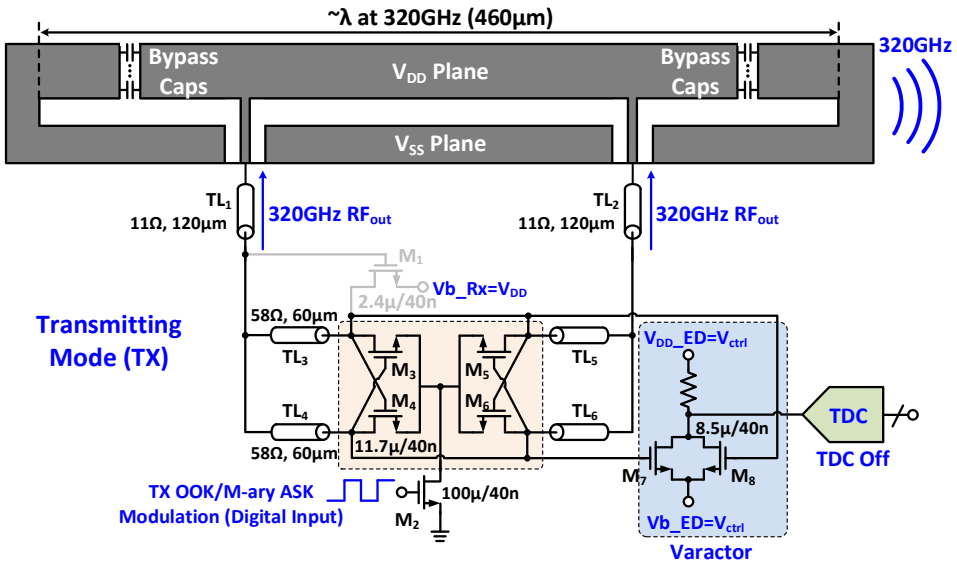

Figure 4.2 – Circuit schematic of the THz pico-radio configured as the transmitter (TX).

In the TX mode, two pairs of cross-coupled oscillators oscillate at f_0=160GHz, and their 2nd harmonic signals ($2f_0$=320GHz) are extracted at the common mode nodes as the THz outputs (Figure 4.2). The cross-coupled transistors M_3–M_6 provide differential negative g_m for oscillation. The transmission lines (T-lines) TL_3–TL_6 on the drain nodes together with the device parasitic capacitors form the resonator tank at f_0=160GHz. The T-lines further perform impedance matching to the on-chip two-feed slot antenna at $2f_0$ to maximize the output power delivered to the antenna, and two in-phase $2f_0$ currents are power-combined directly on the antenna with low loss. The transistors M_7 and M_8 are used as varactors for carrier frequency fine tuning. In the TX mode, the on-chip TDC and the RX injection transistor M_1 are turned off for power saving. For the TX modulation, the OOK/M-ary ASK data drives the tail current source M_2 for direct bits-to-THz transmitting.

The supply voltage of the TX-mode oscillators is 1.1V. In the actual wireless link, the TX output power is optimized based on the system power-performance requirement. As demonstrated in Section 4.3, the TX output power can be backed-off for substantial DC power saving if the radio only needs to cover shorter distances.

4.2.2 On-Chip Antenna

The antenna is integrated on-chip to achieve THz signal radiation and receiving. It is shared between the TX mode and RX mode to save the total radio size. The on-chip antenna is implemented as a two-feed slot antenna, so that the THz signals generated from the two oscillators are in-phase combined on the antenna with low loss [32] [33].

Since the antenna feeds are DC-connected to the drain nodes of the cross-coupled transistor M_3–M_6 (Figure 4.2), it is important to find a low-resistance DC path to provide the supply voltage. One can use an AC-coupled capacitor and a choke inductor as a bias-tee, which is a common practice at MHz/GHz. However, on-chip capacitors exhibit limited self-resonant frequency (SRF) and poor quality factor (Q) at THz, leading to severe THz radiation signal loss and its radiation efficiency degradation.

Alternatively, we choose to feed the supply voltage from the ground plane of the slot antenna by splitting the ground plane to a separate V_{DD} plane and a V_{SS} plane, where the V_{DD} plane provides the DC supply and the V_{SS} plane is DC grounded (Figure 4.3). Sufficient bypass capacitors are needed to ensure electrically short connection between the V_{DD} and the V_{SS} planes to support the desired slot radiation. Since on-chip capacitors have poor Q at THz frequencies, the placement of these capacitors is critical to minimize the loss of the THz radiated signal. We choose to split the antenna ground plane at its natural

surface current null locations and insert the bypass capacitors there. Placing the capacitors at the current nulls naturally minimizes the bypass current going through them and directly reduces their signal loss. Moreover, the high-impedance nature of the surface current null locations allows for the use of only medium-/small-sized capacitors to realize adequate bypassing, so that the capacitor SRF is sufficiently higher than the operating frequency.

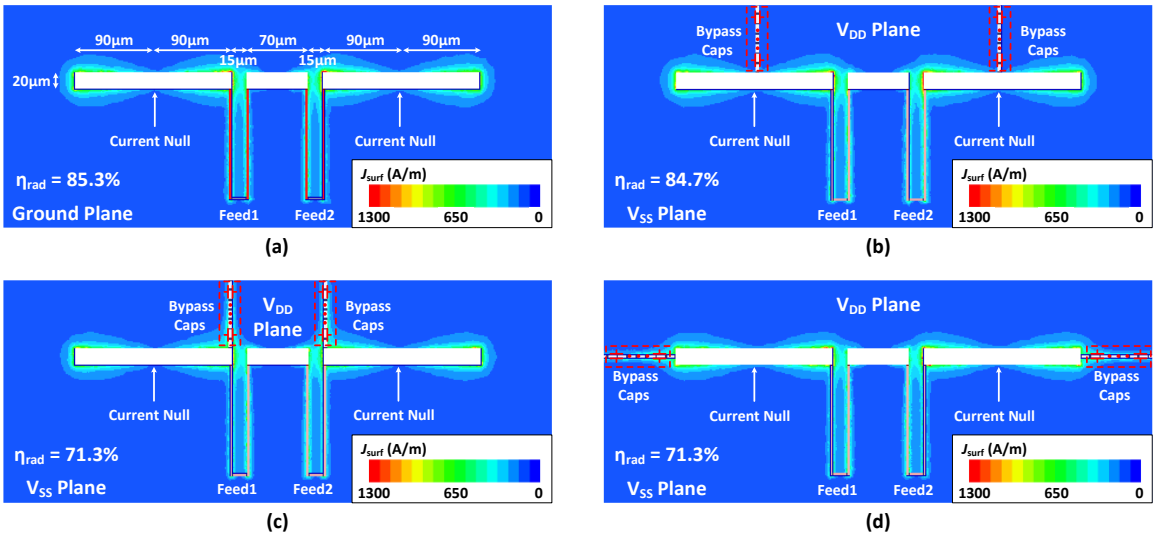

Figure 4.3 – 3D EM-simulated surface current distribution (J_{surf}) and radiation efficiency (η_{rad}) with (a) the natural two-feed slot antenna with an undivided ground plane, (b) capacitors bypassed at the surface current nulls, (c) bypass capacitors placed at the surface current peaks close to the antenna feeds, and (d) bypass capacitors placed at the surface current peaks at the edges of the slot. When the bypass capacitors are inserted at the surface current nulls, the resulting J_{surf} and η_{rad} match well with the case of undivided antenna ground plane, showing that minimal THz signal loss and radiation perturbation are ensured.

The on-chip 320GHz slot antenna is designed with a total length slightly larger than one wavelength (λ). It presents two symmetric surface current null locations, where we split the V_{DD} and V_{SS} planes and insert the supply bypass capacitors for minimal signal loss.

We have simulated the surface current distribution (J_{surf}) and radiation efficiency (η_{rad}) of the two-feed slot antennas for four cases (Figure 4.3). In the 3D EM simulations, the silicon substrate is thinned down to 50μm to enable future vertical stacking with energy harvesting device and maintain a compact radio form factor. The unit bypass capacitor is implemented as a MOM cap with a dimension of 12μm×7μm. The unit bypass capacitor value is 62fF with Q≈10 at 320GHz, and its SRF is more than 450GHz. An array of unit bypass capacitors are placed between the V_{DD} plane and V_{SS} plane to provide a low bypass impedance. The on-chip antenna radiates from the backside of the silicon chip. In case 1, a natural antenna ground plane with no splitting is used as a reference design, showing a simulated η_{rad} of 85.3% [Figure 4.3(a)] as the baseline. The bypass capacitors are inserted at current nulls for the case 2 [Figure 4.3(b)], which achieves almost identical η_{rad} of 84.7% and J_{surf} as case 1. Notably, this case 2 is eventually used in our implementation, and the V_{DD} plane naturally provides the DC supply for the cross-coupled transistors with a very low DC resistance. The bypass capacitors are placed at two other configurations in case 3 [Figure 4.3(c)] and case 4 [Figure 4.3(d)], both yielding a simulated η_{rad} of 71.3%, corresponding to 0.8dB signal loss due to the supply bypass in these two undesired cases.

The SOI process stack up, EM-simulated E-/H-plane patterns at $2f_0$, and return loss at each antenna feed are shown in Figure 4.4. The EM-simulated peak antenna gain is 6.1dBi at 320GHz. We also simulate the antenna behavior at the fundamental frequency 160GHz (Figure 4.5). The EM-simulated peak antenna gain at f_0=160GHz is -1.7dBi with 28.4% radiation efficiency, which is 7.8dB lower than the antenna gain at $2f_0$=320GHz. In addition, since the antenna is fed from the center tap of the differential oscillators, its virtual ground nature at f_0 ensures that there is very little power (-18.6dBc compared to the $2f_0$

tone in the simulation) sent to the antenna. Therefore, the radiation at the fundamental frequency is negligible.

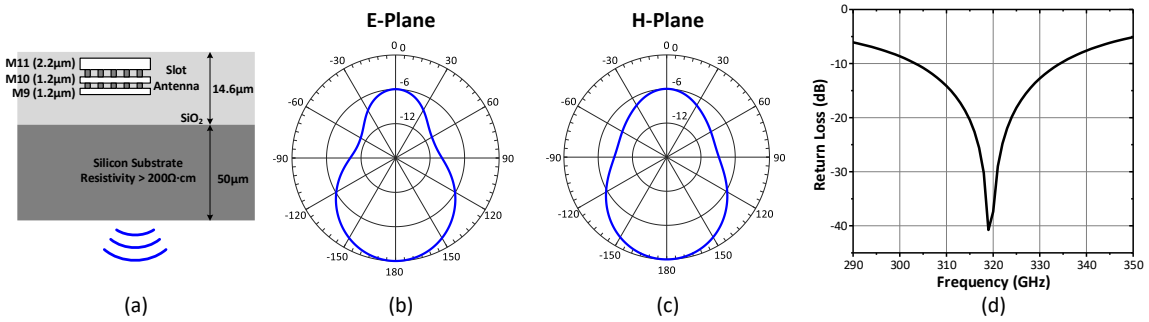

Figure 4.4 – (a) Stack up of the process, (b) EM-simulated E-plane radiation pattern at $2f_0$, (c) EM-simulated H-plane radiation pattern at $2f_0$, and (d) EM-simulated return loss at each antenna feed.

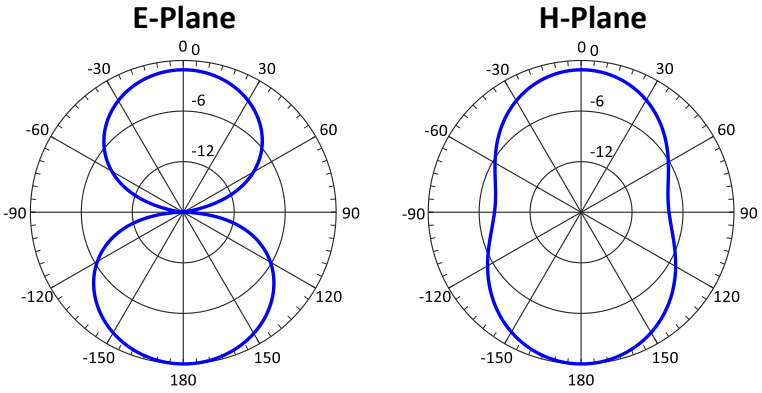

Figure 4.5 – EM-simulated radiation patterns at the fundamental frequency f_0=160GHz.

4.2.3 RX Mode

Existing THz RXs operating above transistor f_{max} can be generally classified as power detector based incoherent detection scheme [84] and sub-harmonic mixer based coherent detection scheme [85]. Conventional passive power detectors feature low DC power consumption, small chip area, and low overhead due to simple supplementary circuits, but they often suffer from poor sensitivity. On the other hand, sub-harmonic

coherent detections often achieve much better sensitivity, especially using a low IF frequency. Coherent detections also provide phase information and support complex quadrature demodulations. Nevertheless, coherent detections require synchronized THz local oscillator (LO) and phase-locked loop (PLL) designs that often lead to large DC power consumption and chip area.

Another incoherent power-based detection approach is to use a super-regenerative receiver (SRR) [88]–[92] that is particularly suitable for field-deployable sensor applications with limited chip area and DC power. SRRs are also popular solutions for GHz low-power RXs and mm-wave/THz imagers [86] [87]. In this work, we propose a super-harmonic super-regenerative RX architecture, where the input signal frequency is around the 2nd harmonic of the oscillation frequency, enabling THz receiving above transistor f_{max}. Moreover, its regenerative nature substantially improves the RX sensitivity over incoherent THz power detectors, and exhibits competitive sensitivity but at significantly lower DC power and smaller chip area compared with coherent sub-harmonic mixer-based RX.

The RX mode operation is explained as follows. Once a $2f_0$ input signal is received by the on-chip antenna, M_1 is turned on, injects a $2f_0$ current into the resonator tank, and creates a small asymmetry to perturb the fundamental oscillation start-up at f_0 (Figure 4.6). The receiving of an OOK-modulated signal is shown as an example, which leads to different RX oscillation start-up times depending on the "0" or "1" received symbol (Figure 4.6). Similarly, M-ary ASK signals can also be received. The transistors M_7 and M_8 are reconfigured as an envelope detector (ED), whose output subsequently triggers the TDC measurement. By periodically quenching the tail current source M_2, the received OOK/M-ary ASK signal is demodulated through measuring and digitizing the regenerative oscillator

start-up time by the TDC, achieving direct THz-to-bits receiving. Notably, the incoherent detection requires oversampling over the symbol rate at the RX to accurately recover the data. In our implementation, a 4× oversampling is chosen for the RX quench signal.

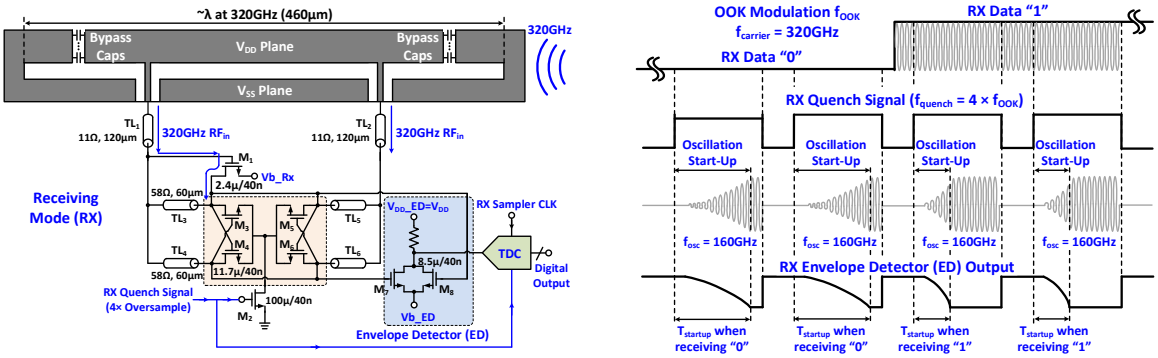

Figure 4.6 – Circuit schematic of the THz pico-radio configured as the receiver (RX). Receiving of OOK-modulated signal is shown as an example.

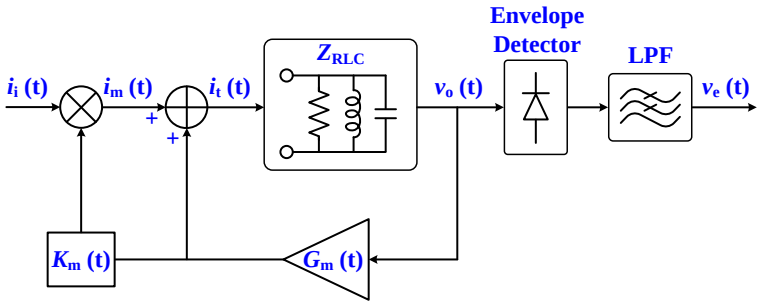

Figure 4.7 – A simplified block diagram of a super-harmonic SRR.

Figure 4.7 shows a simplified generic circuit block diagram to model a super-harmonic SRR. The *RLC* tank Z_{RLC} resonates at the fundamental frequency ω_0. $G_{\mathrm{m}}(t)$ is the equivalent transconductance of the oscillator. The mixing operation due to the oscillator nonlinearity is modeled as a mixer, and $K_{\mathrm{m}}(t)$ models the gain of the nonlinear feedback block. $v_{\mathrm{o}}(t)$ is the transient oscillator output, while $v_{\mathrm{e}}(t)$ is the filtered envelope of the oscillator output. The external signal injected around the 2$^{\mathrm{nd}}$ harmonic frequency is

modeled as a current source $i_{\mathrm{i}}(t) = I_{\mathrm{i}} \cos(\omega_{\mathrm{i}} t)$ with $\omega_{\mathrm{i}} \approx 2\omega_0$. The quiescent damping factor of the *RLC* tank [90] [91] is defined as

$$\zeta_0 = \frac{\omega_0 L}{2R} = \frac{1}{2\omega_0 RC} . \tag{4.1}$$

Using the block diagram shown in Figure 4.7, the 2nd order differential equation to describe the system can be written as

$$v_{\mathrm{o}}''(t) + 2\zeta_0 \omega_0 v_{\mathrm{o}}'(t) + \omega_0^2 v_{\mathrm{o}}(t) = 2R\zeta_0 \omega_0 i_{\mathrm{t}}'(t) , \tag{4.2}$$

where $i_{\mathrm{t}}(t)$ is expressed as

$$i_{\mathrm{t}}(t) = i_{\mathrm{m}}(t) + G_{\mathrm{m}}(t) v_{\mathrm{o}}(t) . \tag{4.3}$$

Substituting (4.3) into (4.2) results in

$$\begin{aligned} v_{\mathrm{o}}''(t) + 2\zeta(t)\omega_0 v_{\mathrm{o}}'(t) + \omega_0[\omega_0 - 2R\zeta_0 G_{\mathrm{m}}'(t)] v_{\mathrm{o}}(t) \\ = 2R\zeta_0 \omega_0 i_{\mathrm{m}}'(t) , \end{aligned} \tag{4.4}$$

where $\zeta(t)$ is the instantaneous damping factor, as

$$\zeta(t) = \zeta_0 [1 - G_{\mathrm{m}}(t) R] . \tag{4.5}$$

Assuming $\zeta(t)$ varies much slower with respect to ω_0, i.e., $\zeta'(t) \ll \omega_0$ [92], then (4.4) can be simplified as

$$v_{\mathrm{o}}''(t) + 2\zeta(t)\omega_0 v_{\mathrm{o}}'(t) + \omega_0^2 v_{\mathrm{o}}(t) = 2R\zeta_0\omega_0 i_{\mathrm{m}}'(t)\,, \tag{4.6}$$

where $i_{\mathrm{m}}(t)$ is defined as

$$i_{\mathrm{m}}(t) = K_{\mathrm{m}}(t)G_{\mathrm{m}}(t)v_{\mathrm{o}}(t)i_{\mathrm{i}}(t) = K_{\mathrm{m}}(t)G_{\mathrm{m}}(t)v_{\mathrm{o}}(t)I_{\mathrm{i}}\cos(\omega_{\mathrm{i}}t)\,. \tag{4.7}$$

After the quench signal is turned on, the instantaneous damping factor $\zeta(t)$ becomes negative, and the transistors provide more energy to overcome the loss in the resonant tank, so the oscillation builds up. When the quench signal is turned off, the damping factor $\zeta(t)$ becomes positive, meaning that the oscillation cannot be sustained and quickly dies out. The general solution of (4.6) consists of free response and forced response. By periodically turning on and off the quench signal, any oscillation from a previous cycle is quenched before a new cycle starts, so the free response is zero, and the solution of (4.6) is purely determined by the excitation, i.e., the received signal $i_{\mathrm{i}}(t)$ at the $2\omega_0$.

Comparing (4.6) for the proposed super-harmonic SRR with the 2nd order differential equation for a conventional SRR [90]–[92], the difference is that a conventional SRR takes the excitation at the fundamental frequency ω_0, but in the super-harmonic SRR, the excitation $i_{\mathrm{m}}(t)$ is the mixing term of the input received signal $i_{\mathrm{i}}(t)$ at $\omega_{\mathrm{i}} \approx 2\omega_0$ with the oscillator output $v_{\mathrm{o}}(t)$ at ω_0, which presents a mixing tone close to ω_0 after the *RLC* filtering. Therefore, existing operation theories developed for SRR can be applied here to analyze the proposed super-harmonic SRR. To fully utilize the nonlinearity of the oscillator and facilitate the generation of the $(\omega_{\mathrm{i}} - \omega_0)$ mixing term, our super-harmonic SRR is designed to work in the logarithmic mode. This improves the RX sensitivity by the enhanced mixing term and extends its RX dynamic range using time-encoded output [86].

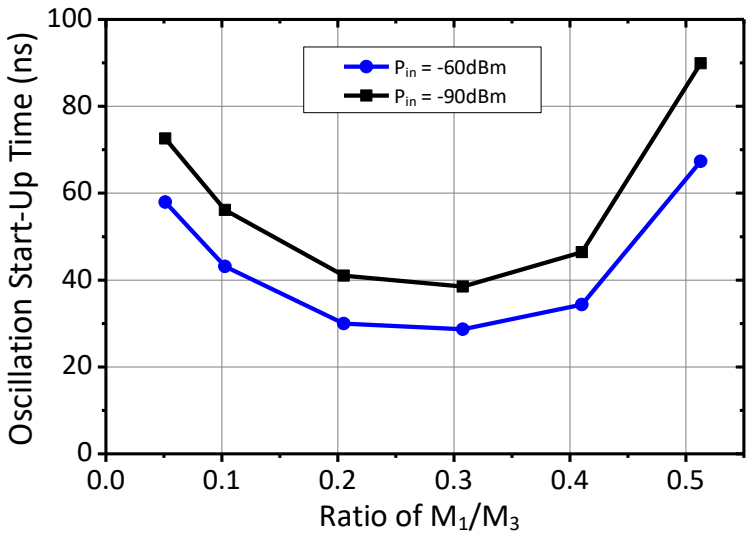

Figure 4.8 – Simulated RX oscillation start-up time versus the size ratio of M_1/M_3 with P_{in}=-60dBm/-90dBm.

The size of the input injection transistor M_1 deserves careful considerations. First, if M_1 is removed, meaning that the oscillator is completely symmetrical with the center tap connected to the antenna feeds, the oscillation start-up time does not show significant change with and without input power at $2f_0$ in simulations. Therefore, the small asymmetry introduced by M_1 is important for the desired super-harmonic SRR operation. However, if the size of M_1 is too large, it degrades the 2nd harmonic generation efficiency and fundamental leakage suppression in the TX mode. It also hurts the differential oscillation due to significant asymmetry. On the other hand, if M_1 is too small, the oscillation start-up time becomes less sensitive to the input power level and vulnerable to process variation. The RX oscillation start-up time versus the size ratio of M_1/M_3 with P_{in}=-60dBm/-90dBm is shown in Figure 4.8. In our implementation, the size ratio is chosen as 0.2 and M_1 is implemented as 2.4µm/40nm with 3 fingers. The simulated transient oscillation waveforms at different input power levels are shown in Figure 4.9, representing receiving an OOK or M-ary ASK modulated signal. The RX oscillation start-up time gradually decreases with

larger received input power, and the time-encoded output is readily resolved and digitized by an on-chip low-power TDC.

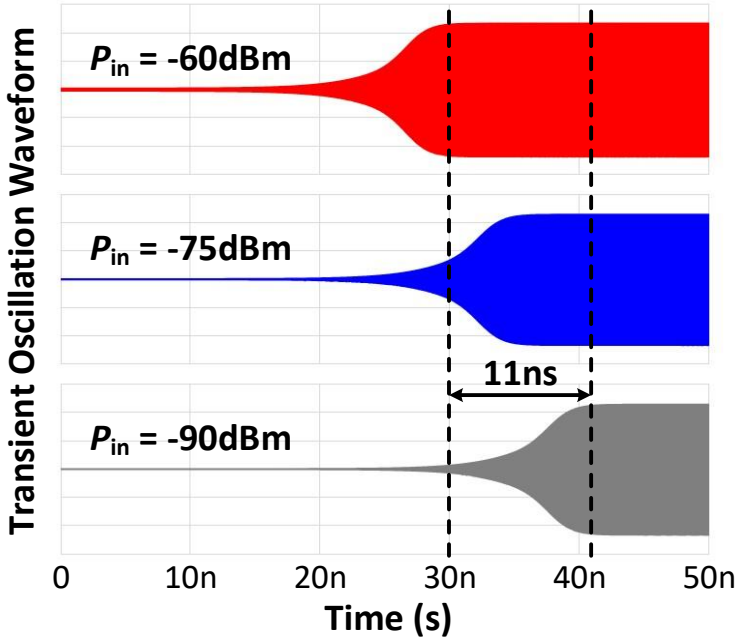

Figure 4.9 – Simulated transient oscillation waveforms at different input power levels, representing the received OOK or M-ary ASK modulated signal. The RX oscillation start-up time gradually decreases with larger input power, and the time-encoded output is resolved by an on-chip low-power TDC.

4.2.4 Time-to-Digital Converter (TDC)

Based on the proposed super-harmonic SRR operation (Figure 4.9), a fine TDC timing resolution (~ tens of ps) is critical to achieve high RX sensitivity, whilst a large detectable timing range (~ tens of ns) is needed to capture the entire regenerative oscillation start-up event. These two timing requirements pose challenges for conventional TDCs, and judicious design considerations are thus required.

Our TDC is designed as a 2-step TDC with a coarse TDC and a fine TDC (Figure 4.10), achieving large conversion range and fine timing resolution simultaneously [93].

The coarse TDC is implemented as a sampler with a timing resolution of 500ps, while the fine TDC is implemented as a 2D Vernier structure, covering a 725ps conversion range with a timing resolution of 25ps. The 2D Vernier TDC [93] [94] comprises two slightly different delay lines and a 2D comparator array, presenting several unique advantages. First, compared with conventional single inverter-delay-line based TDC (flash TDC) [95] that quantizes time information based on the propagation delay of each individual inverter, the Vernier TDC has a greatly improved timing resolution that is determined by the propagation delay difference of the unit delay cells in the two delay lines, i.e., τ_s-τ_f (Figure 4.10) Secondly, the Vernier delay line architecture is less sensitive to process-voltage-temperature (PVT) variations since the 1st order PVT mismatches are automatically cancelled if the two delay lines are well matched [96]. Monte Carlo simulations for the fast delay (τ_f), slow delay (τ_s), and delay difference (τ_s-τ_f) are shown in Figure 4.11(a), and the PVT dependence is illustrated in Figure 4.11(b). Both results indicate a significant improvement on the robustness to PVT variations for the Vernier delay line. In addition, by using a 2D comparator based Vernier TDC, the number of delay stages can be substantially reduced for further power saving [94] [97].

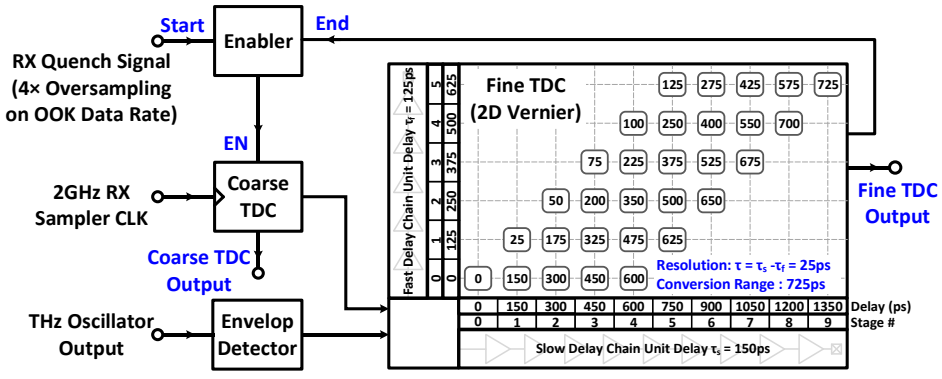

Figure 4.10 – Circuit schematic of the on-chip low-power TDC.

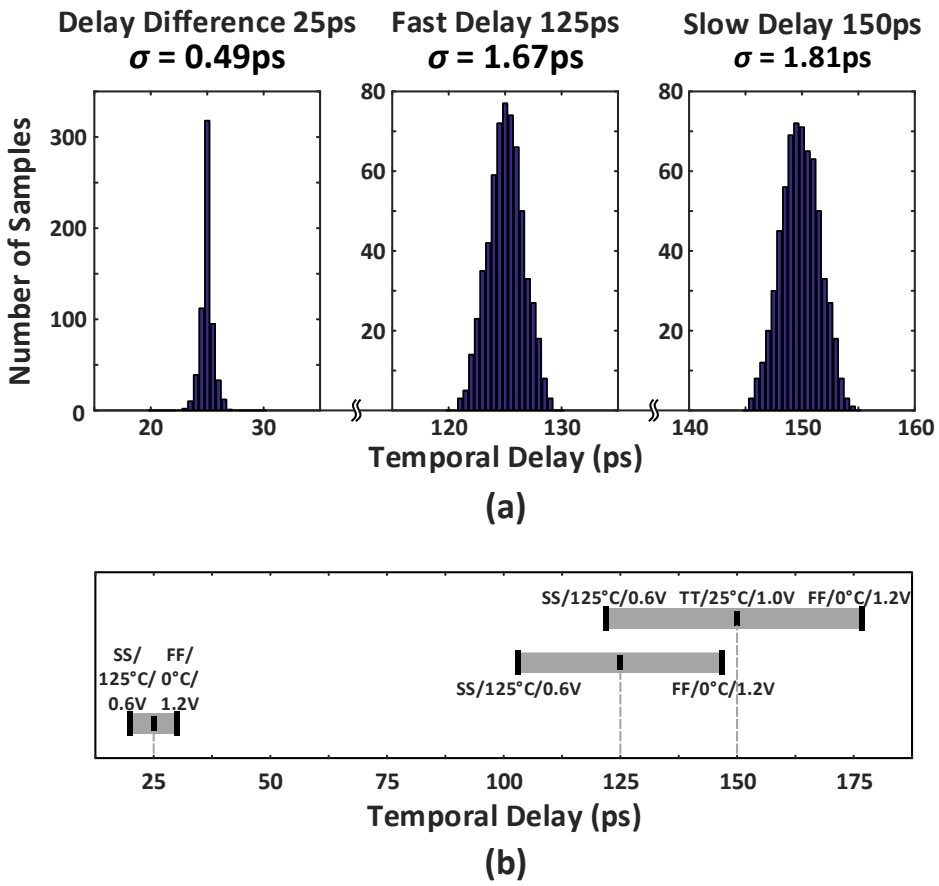

Figure 4.11 – (a) Monte Carlo simulations of the fast delay (τ_f), slow delay (τ_s) and delay difference (τ_s-τ_f) on the process variations. (b) Simulated delay variations over temperature, supply voltage and corners.

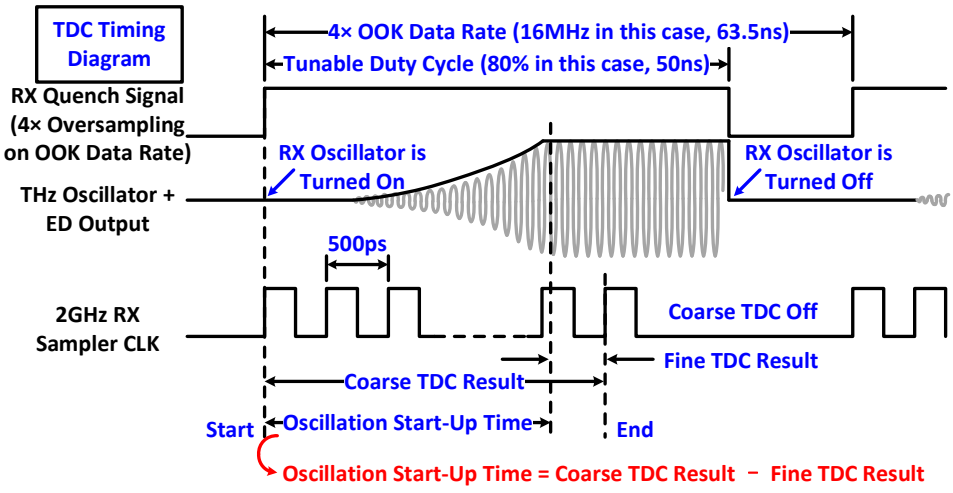

Figure 4.12 – Timing diagram of the RX mode and the TDC, assuming 4Mb/s OOK data rate.

The timing diagram of the RX mode and TDC is explained as follows. Once the RX quench signal turns on the THz regenerative oscillator, its start-up time is first sampled by the coarse TDC. The ED output rises in proportion to the oscillator growing amplitude, and it eventually passes a threshold and triggers the fine TDC. The fine TDC then resolves the time interval of the coarse TDC residue, i.e., the timing difference between the onset of the fine TDC and the immediate next clock edge of the coarse TDC (Figure 4.12). The RX oscillation start-up time is thus the output difference of the coarse and fine TDCs. At low data rate, the duty cycle of the quench signal is reduced to further save the RX DC power.

4.3 Measurement Results

The bidirectional THz pico-radio is designed and fabricated in a 45nm CMOS SOI process with a high-resistivity substrate (Figure 4.13). The miniaturized THz pico-radio only occupies 950×600μm^2 including all the pads. The CMOS chip is wire-bonded to a PCB to facilitate the testing. The measurement results of the TX mode, on-chip TDC, RX mode, and wireless communication links are presented in this section.

4.3.1 TX Mode Characterization

The TX mode of the THz pico-radio is characterized first. The TX output is received by a diagonal horn antenna, and then down-converted by a VDI WR2.8 even harmonic mixer (EHM). The EHM uses the 20th harmonic of an external LO provided by a signal generator. After frequency down-conversion, the IF output is amplified by an IF amplifier and captured with a spectrum analyzer (Figure 4.14). Due to the limited power generated from the TX mode, the Erickson power sensor does not have enough sensitivity

to measure the absolute power from the TX at the far-field. Therefore, the output power from the TX mode is measured by the setup shown in Figure 14. The conversion loss of the EHM is calibrated using an R&S 220-330GHz frequency extender. A typical output spectrum after down-conversion is shown in Figure 4.15.

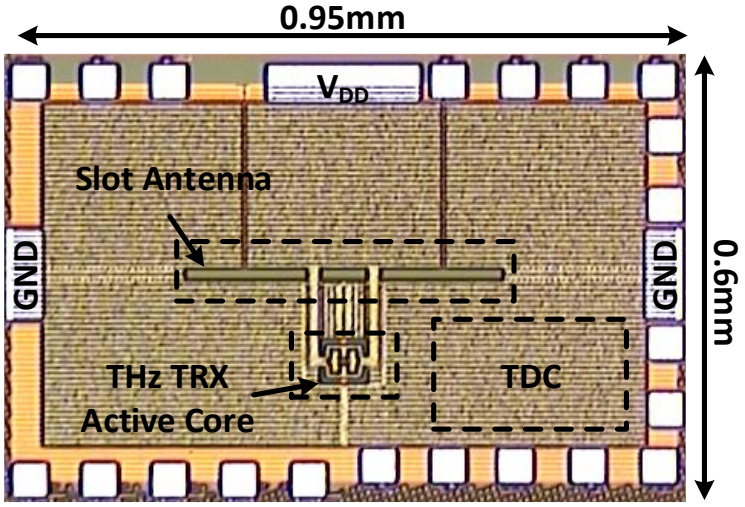

Figure 4.13 – THz pico-radio chip microphotograph.

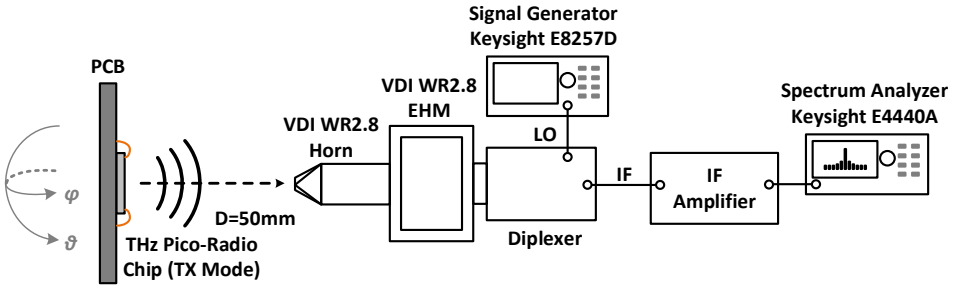

Figure 4.14 – THz pico-radio TX mode measurement setup.

We first measure the received power ($P_{received}$) by the horn antenna versus the distance between the TX and the horn antenna (Figure 4.16). When the distance is larger than 5cm, the measured $P_{received}$ matches well with the Friis transmission equation, indicating far-field condition [1]. Therefore, a distance of 5cm is chosen for all the subsequent TX characterization. The measured frequency tuning for three independent

samples is shown in Figure 4.17. The TX frequency is tunable from 316 to 321GHz, and the maximum frequency difference among three samples is only 1.2GHz, verifying design robustness. The Equivalent Isotropically Radiated Power (EIRP) versus DC power and the DC-to-EIRP efficiency are shown in Figure 4.18. The measured TX peak EIRP is -11.6dBm with a peak 0.19% DC-to-EIRP efficiency at 36.3mW TX DC power.

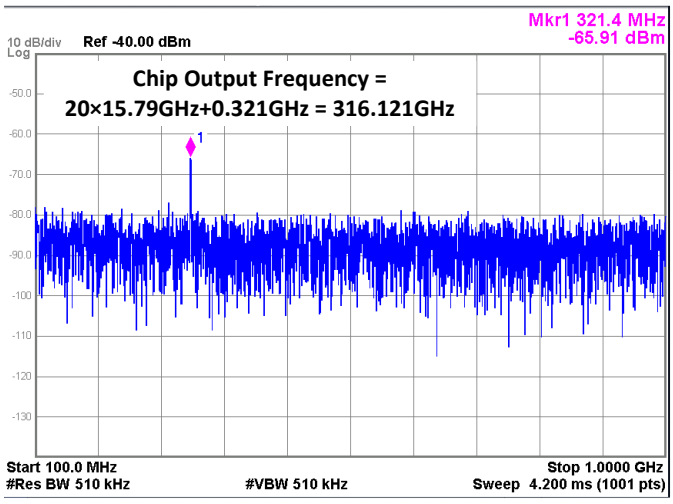

Figure 4.15 – A typical measured output spectrum after down-conversion by the 20th harmonic signal of the LO.

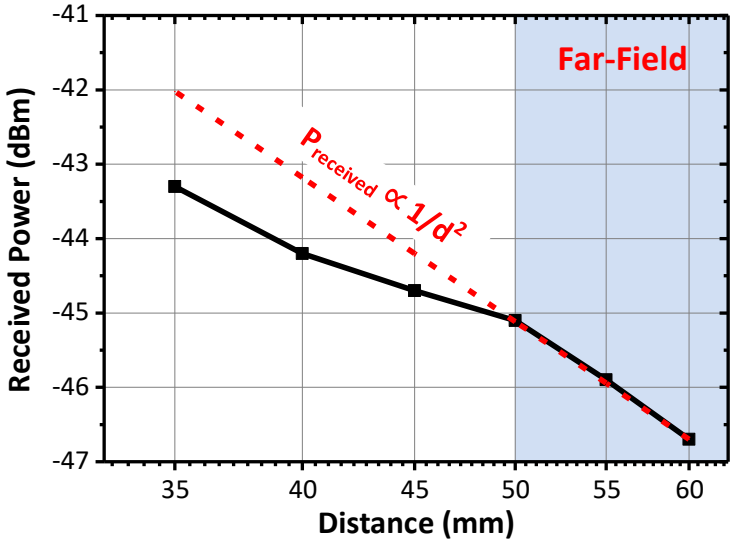

Figure 4.16 – The received power ($P_{received}$) by the horn antenna at 316GHz versus the distance between the TX and the horn antenna, verifying the far-field radiation.

The two-feed slot antenna shown in Section 4.2.2 is designed using 50µm substrate thickness to enable vertical stacking with energy harvesting/storage devices and maintain a compact radio form factor. In this boundary condition, it is assumed that the energy harvesting device is attached at the frontside of the chip, and the on-chip antenna radiates from the backside. However, since this paper does not present the full integration of the THz pico-radio with the energy harvesting/storage devices, we choose not to thin the substrate (230µm) and the chip is directly attached to the ground plane of the PCB in our proof-of-concept measurements. The antenna radiates from the frontside of the chip. Chip backside grinding and flip-chip (or other) packaging technologies will be employed when the THz pico-radio is integrated with the energy harvesting/storage devices.

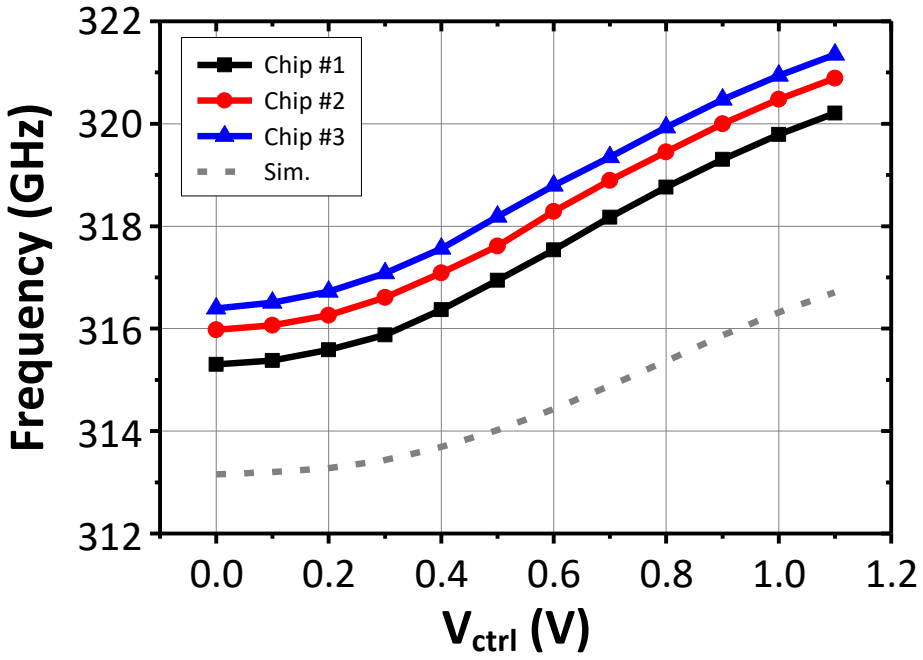

Figure 4.17 – Measured TX frequency tuning ranges for three independent samples.

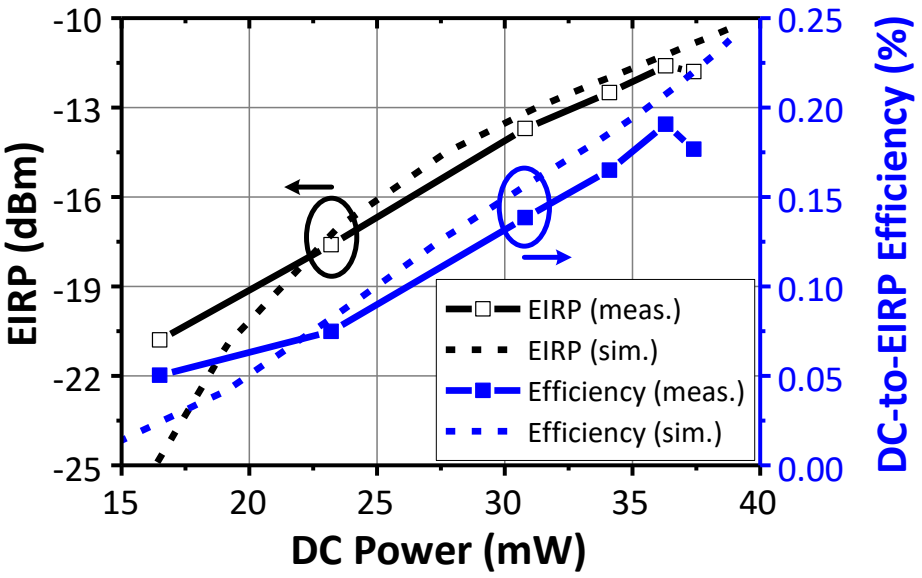

Figure 4.18 – Measured TX EIRP versus DC power consumption, and calculated DC-to-EIRP efficiency.

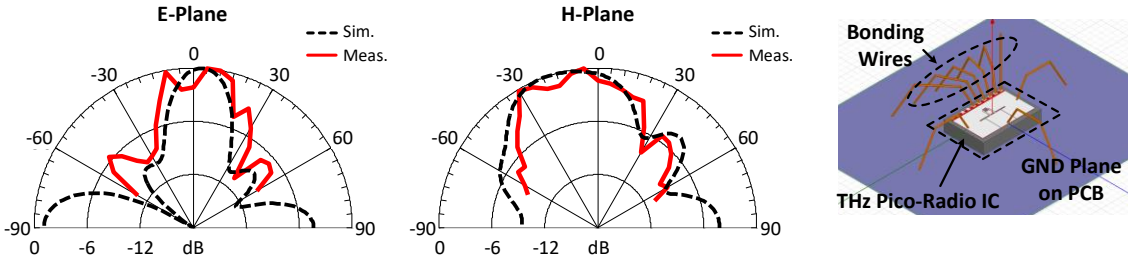

Figure 4.19 – Measured E-/H-plane radiation patterns at 316GHz and 3D EM simulation setup for frontside radiation without substrate grinding.

To clarify this boundary condition difference, we have plotted the EM-simulated together with measured antenna patterns for the frontside radiation in Figure 4.19. The 3D EM simulation setup is also shown in Figure 4.19. The radiation patterns are measured by rotating the TX PCB in the elevation (θ) and azimuth (φ) directions. The antenna radiation patterns are distorted due to the thicker substrate and close-in bonding wires in this frontside simulation setup and its measurement results. The EM-simulated peak antenna gain also decreases from 6.1dBi to -1.1dBi.

Knowing that the frontside radiation setup has comprised performance, we use such a setup just to demonstrate the communication functionalities of our THz pico-sized radio. Preferred backside radiation will be employed in our future studies with integration of energy harvesting/storage devices. We also expect that the backside radiation will improve the communication distance by about 4× due to the antenna gain improvement for both TX and RX.

4.3.2 TDC Characterization

Next, the on-chip low-power TDC is characterized. In a 2-step TDC, minimizing the gain difference between the coarse and fine TDCs are critical, since any gain mismatch leads to a nonlinear TDC conversion. Thus, an on-chip automatic calibration system was built to adjust the fine TDC transfer curve to match the gain of the coarse TDC for its linearity improvement [98]. Table 4.1 summarizes the main specifications of the 2-step TDC, covering a conversion range from 0 to 63.5ns with a resolution of 25ps. The measured TDC transfer curves with and without the automatic calibration are shown in Figure 4.20(a) with a zoom-in view in Figure 4.20(b). The gain mismatch is suppressed after the auto-calibration, indicating a linear conversion.

Table 4.1 – TDC performance summary.

	Structure	Resolution	Range	DC Power
Coarse TDC	Sampler	500ps	7-bit	0.5mW
Fine TDC	2D Vernier	25ps	5-bit	0.25mW

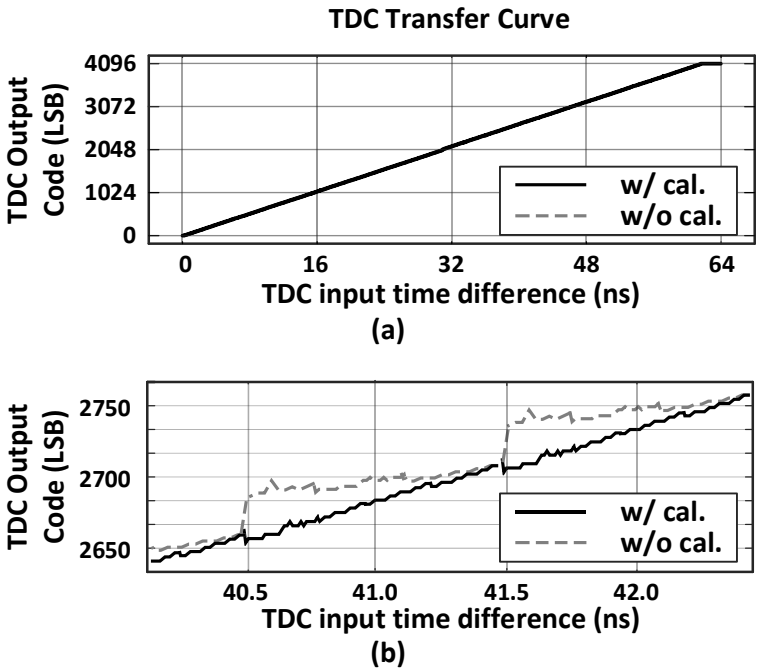

Figure 4.20 – (a) Measured TDC transfer curves with and without the automatic calibration. (b) A zoom-in view of the TDC transfer curves.

4.3.3 RX Mode Characterization

For the RX mode measurement, an R&S 220-330GHz frequency extender with a horn antenna is used to transmit a single-tone continuous-wave (CW) signal to the RX chip. The TDC digital output is monitored using a mixed-signal oscilloscope (Figure 4.21). During the measurement, the frequency extender is turned on and off, and the RX oscillation start-up time difference is recorded (Figure 4.22). At each frequency point, 100 measurement results are collected to compute the mean and standard deviation of the RX oscillation start-up time. The super-harmonic SRR bandwidth is defined as the frequency range over which the RX oscillation start-up time changes by 50% for a constant RX received power $P_{received}$ [86]. In this case, the measured RX bandwidth is from 316 to 324GHz (Figure 4.22).

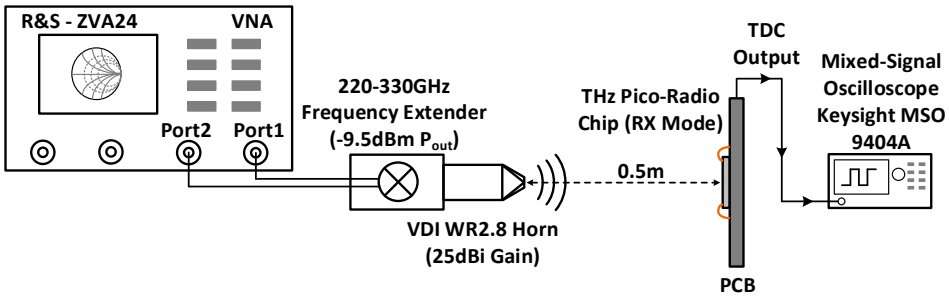

Figure 4.21 – THz pico-radio RX mode measurement setup.

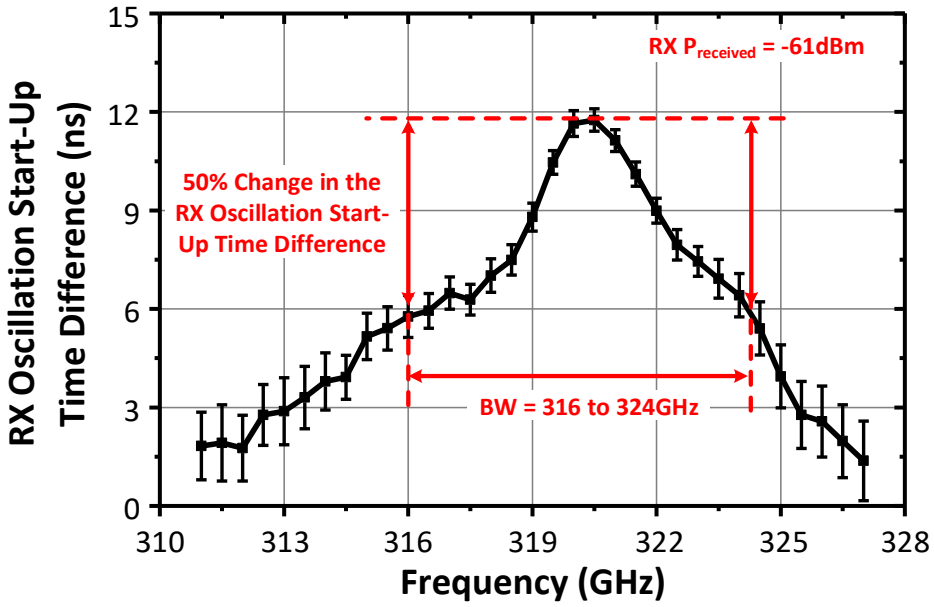

Figure 4.22 – The RX oscillation start-up time difference with/without the input tone versus RX input frequencies. 100 measurements are collected at each frequency point to calculate the mean and standard deviation of the super-harmonic SRR oscillation start-up time.

4.3.4 THz Pico-Radio Link Characterization Using CW Signals

After characterizing the individual performance of the TX and RX, two THz pico-radio chips are used as a TX/RX pair to establish a low-power THz wireless link. We first perform the continuous-wave (CW) link measurements, where the RX oscillation start-up time is measured versus the TX/RX distance and TX EIRP set by the TX DC power

consumption, shown in Figure 4.23(a). At each TX/RX distance and TX DC power setting, 50 measurements are collected to compute the mean and standard deviation of the RX oscillation start-up time. When the TX is off, the RX oscillation start-up time is measured as43.1±1.07ns. For a given TX DC power, the RX oscillation start-up time increases for larger TX/RX distances, due to the reduced THz power received by the RX. For a fixed TX/RX distance, the RX oscillation start-up time increases when TX power is backed-off, also due to the reduced received signal strength. The maximum CW link distance is 55cm at 36.3mW TX DC power. The RX sensitivity is extracted as -89dBm using the measured TX EIRP and the path loss. Typical measured RX start-up timing histograms are also shown in Figure 4.23(b).

4.3.5 THz Pico-Radio Link Demonstration Using OOK Signals

Next, a reliable high-quality wireless communication based on OOK modulation is established between the two THz pico-radio chips. The measured data rate, TX/RX distance, and TRX total DC power consumption are summarized in Figure 4.24. The maximum data rate of 4.4Mb/s (BER<10^{-7}) over 50cm maximum TX/RX distance is supported at a peak TRX DC power of 49.3mW.

In all the measurements, a 4× oversampling is used and the maximum duty cycle for the RX quench cycle is 80%. As shown in Figure 4.23, when TX is turned off, the RX oscillation start-up time is around 43.1ns. Therefore, the maximum symbol rate without significant BER is estimated as 1/4/43.1n×80%=4.6Msym/s, which aligns with our measurement results.

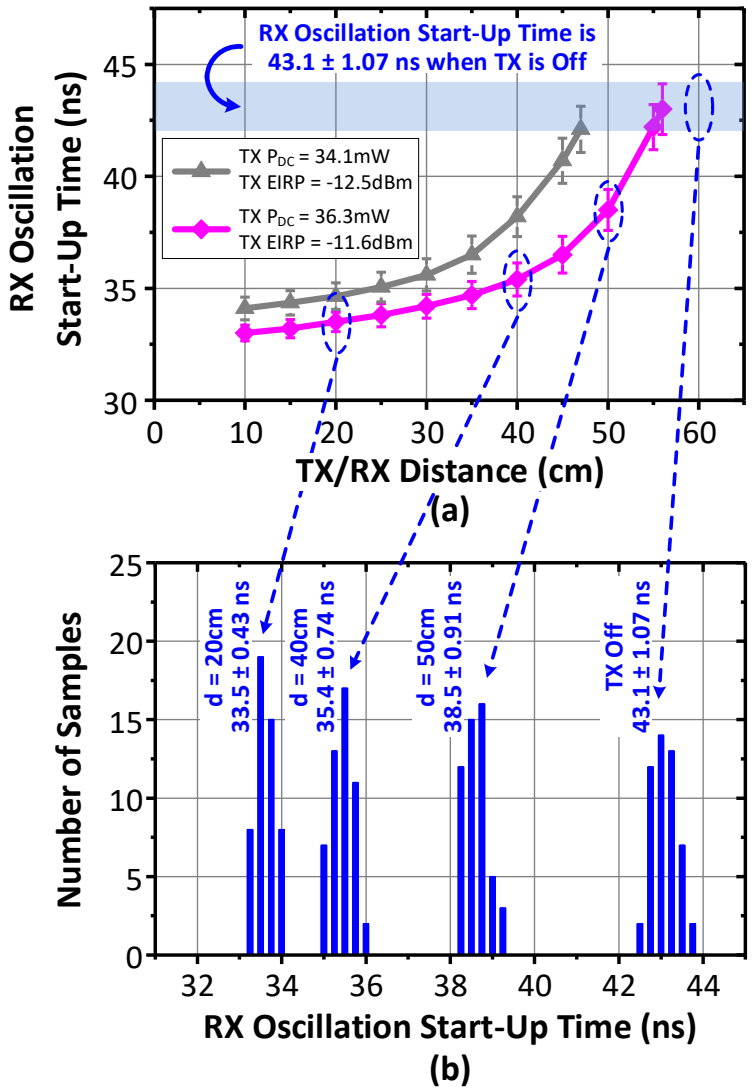

Figure 4.23 – THz pico-radio CW communication link characterization results, including (a) the measured RX oscillation start-up time versus TX/RX communication distance at different TX DC power, and (b) typical measured RX start-up timing histograms at 36.3mW TX DC power with 50 measurement results collected at each communication distance.

The THz pico-radio TRX achieves power-performance scalable operation, where the radio DC power is optimized based on the actual link distance and data rate [Figure 4.24(a)]. The TX DC power and its output power can be lowered for closer communication distances, while RX quench signal duty cycle can be reduced for lower data rates. For example, the TRX total DC power reduces to 26.4mW when the data rate is lowered to

1Mb/s while keeping 50cm TX/RX distance. The TRX DC power further reduces to 18.7mW with 1Mb/s data rate when the communication distance is set at 17cm.

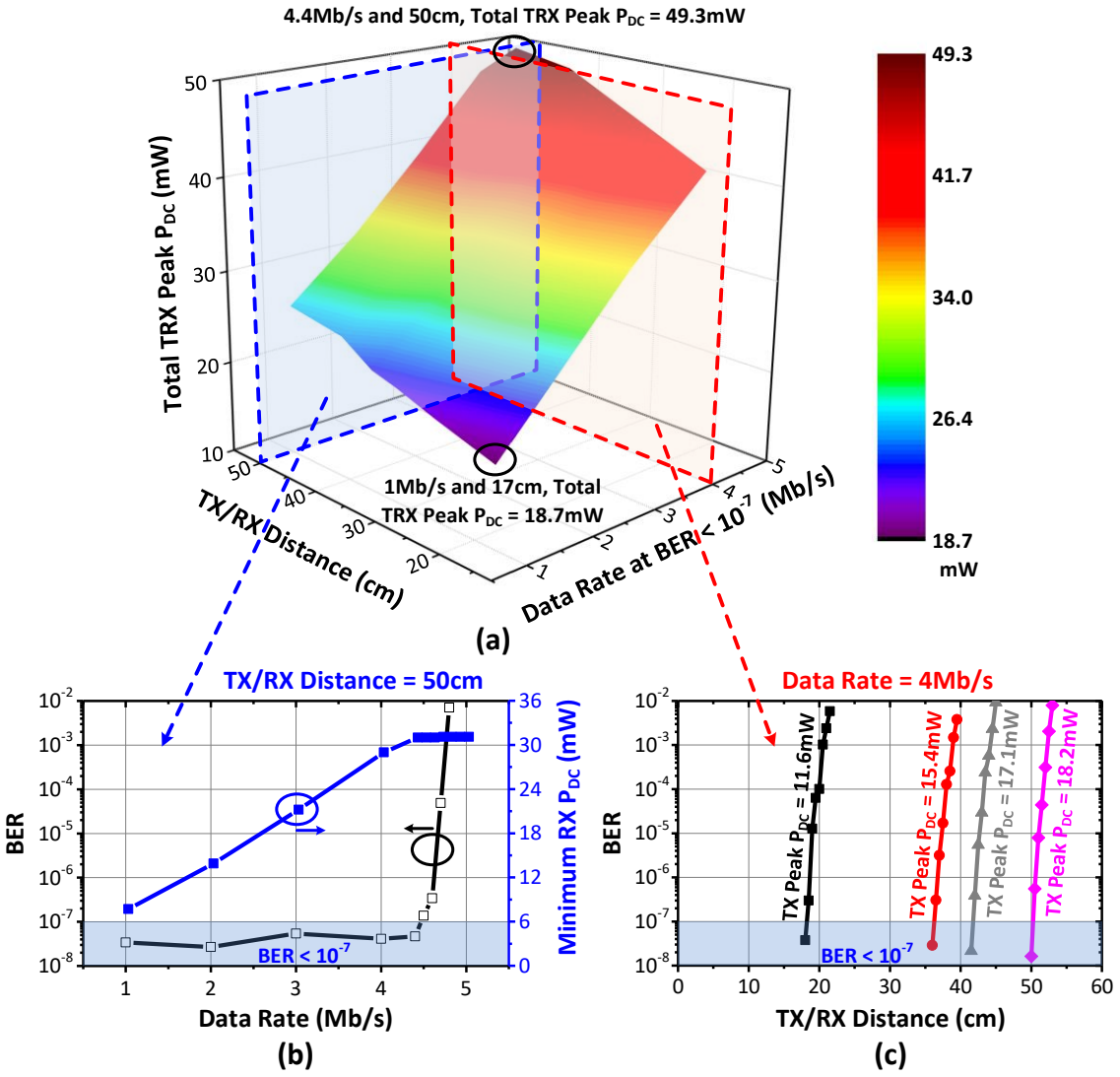

Figure 4.24 – THz pico-radio wireless communication link using OOK modulations. (a) The results are summarized as measured TRX peak DC power versus TX/RX communication distance and OOK data rate at BER<10^{-7}. (b) Measured BER and minimum RX DC power versus data rate over a fixed TX/RX distance of 50cm. (c) Measured BER versus TX/RX distance at different TX DC power for 4Mb/s OOK signals.

The measured BER and minimum RX DC power versus data rate over a 50cm communication distance is shown in Figure 4.24(b). In addition, the measured BER versus

TX/RX distance at different TX DC power for 4Mb/s OOK signals is shown in Figure 4.24(c).

4.3.6 THz Pico-Radio Link Demonstration Using M-ary ASK Signals

With the high-resolution on-chip TDC, the RX is also able to accurately distinguish the received signal strength based on the oscillation start-up time at a fixed TX/RX distance (Figure 4.23). Therefore, two THz pico-radio chips are used to establish an M-ary ASK based wireless link to increase the total communication throughput. The measured maximum communication distance versus number of bits/symbol for M-ary ASK modulations are shown in Figure 4.25. The demonstrated ASK link supports maximum 16Mb/s 4-bit 16-ary ASK communication over 17cm with BER<10^{-5}. The high-quality wireless link and low BER outperform many reported low-power radios (Table 4.2).

For the TX output power, when more control bits for the TX biasing current source are turned off, the TX EIRP decreases accordingly; this is equivalent to the low AM amplitude in an M-ary ASK modulation. Therefore, with a given RX sensitivity, the maximum TX/RX communication distance of the M-ary ASK modulation is limited by the symbol uses the lowest AM amplitude in the M-ary ASK modulation. This aligns with the measurement results shown in Figure 4.25. Therefore, the major advantage of using M-ary ASK modulation is to achieve a higher data rate, while the disadvantage is that the maximum TX/RX distance is reduced.

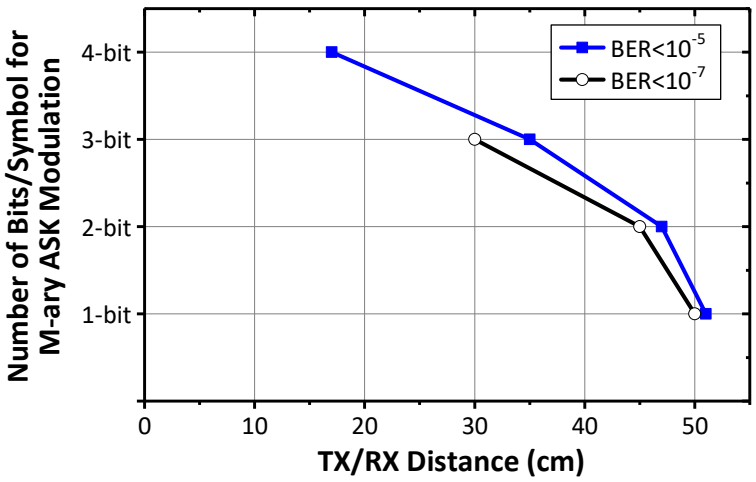

Figure 4.25 – THz pico-radio communication link using M-ary ASK modulations with a symbol rate of 4Msym/s. The results are summarized according to the maximum communication distance versus the number of bits/symbol.

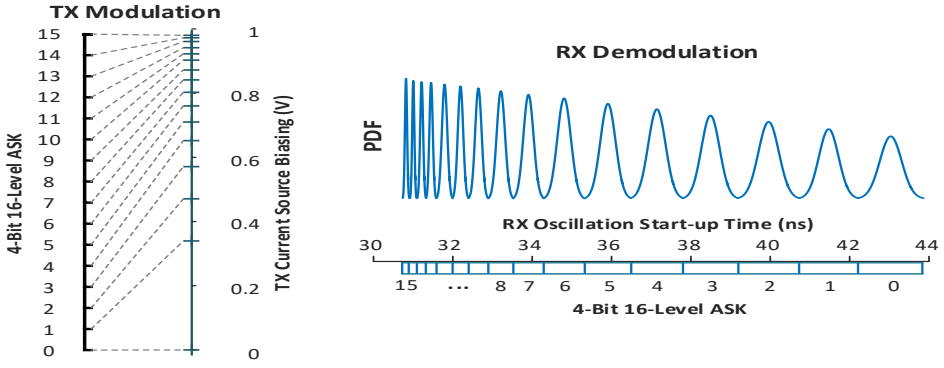

Figure 4.26 – Nonlinear mapping between the amplitude levels and TX current source biasing for the TX modulation, and nonlinear mapping between the amplitude levels and RX oscillation start-up time for the RX demodulation, using 4-bit ASK modulation with 17cm TX/RX distance as an example.

As the RX oscillation start-up time variation gradually increases when the RX input power decreases, a nonlinear mapping between the amplitude levels and TX current source biasing is required for the TX modulation, and another nonlinear mapping between the amplitude levels and RX oscillation start-up time is required for the RX demodulation. These nonlinear mappings are generated based on the CW communication link

measurement results (Figure 4.23). An exemplar nonlinear mapping of 4-bit 16-level ASK communication with 17cm TX/RX distance is shown in Figure 4.26.

Besides wireless communication, this capability of accurately distinguishing received THz signal amplitude can be used to monitor the real-time THz transmission characteristics between the TX/RX pair; this will enable a wide variety of distributed sensing applications, such as very-large-scale position/motion tracking, THz-range temperature/humidity monitoring, vibration/deformation sensing, or non-contact THz electromagnetic "tactile sensing".

4.4 Chapter Summary

This chapter reports an exploratory study on using CMOS low-power THz radios to support high-quality short-range wireless link. A THz pico-radio concept is proposed that achieves extreme radio miniaturization to enable future "invisible" field-deployable sensor network and IoT applications. The bidirectional TX/RX circuit sharing architecture configures the THz pico-radio as an OOK/M-ary ASK-modulated harmonic oscillator in the TX mode or as a super-harmonic SRR with high sensitivity at significantly reduced DC power than conventional coherent down-conversion RX. A low-power TDC is integrated on-chip to directly convert and digitize RX outputs, minimizing the post signal processing.

Compared with the reported Si-based 300GHz TRXs, this bidirectional THz pico-radio achieves the lowest maximum DC power (49.7mW) and the longest communication distance (50cm) without any silicon lens (Table 4.2). Compared with reported low-power radios at MHz, GHz, and mm-wave frequencies, it also achieves the highest radio miniaturization (>7.8× radio size reduction), highest data rate (maximum 16Mb/s 16-ary

ASK signals with BER<10^{-5}), best energy/bit FOM, and competitive DC power consumption (Table 4.2). The reported TX/RX power consumption is the peak DC power during the radio operation. Heavily duty-cycled operations, typical for low-power sensor nodes and IoT devices, will substantially reduce the average DC power of the proposed THz pico-radio down to µW level.

Table 4.2 – Comparison with state-of-the-art THz transceivers and MHz/GHz/Mm-wave low-power radios.

	This Work		VLSI 11	TMTT 16	JSSC 14	ISSCC 16	ISSCC 17	ISSCC 13	JSSC 15
Frequency (GHz)	**320**		380	240	210	0.112 (TX) 0.05 (RX)	0.915	9.8	60 (TX) 24(RX)
Radio Size (mm^2)	**0.57 (TRX+Ant.)**		4.18 (TRX+Ant.)	1.70 (TX+Ant.) 1.57 (RX+Ant.)	3.5 (TX+Ant.) 1.12 (RX+Ant.)	2.22 (TRX) + 8 (Ant.)	9 (TRX+Ant.)	2.73 (TRX) + 1.95 (Ant.)	4.44 (TRX+Ant.)
TX EIRP (dBm)	**-11.6**		-13	21.9 (w/ Si Lens)	5.1	-78 at 50cm	-26.9	0.1	-6.5
RX Sensitivity (dBm)	**-89**		-40†	-60†	-64†	-54 at 100kb/s	-93	-77	-10.5
Peak DC Power (mW)	**18.2 (TX)***	**26.1 (TX)***	364 (TRX)	1033 (TX)	240 (TX)	13.6 (TX)	2 (TX)	0.291 (TX)	N/A
	31.1 (RX)*	**31.1 (RX)***		886 (RX)	68 (RX)	0.036 (RX)	1.85 (RX)	0.306 (RX)	
Max. Communication Distance (cm)	**50**	**17**	10	15	3.5	50 (TX) 20 (RX)	2000	250	50
Data Rate and Modulation Type	**4.4Mb/s OOK**	**16Mb/s 4-bit ASK**	Chirp	2.73Gb/s QPSK	CW	2kb/s PPM	30kb/s M-ary PPM	30kb/s PPM	12Mb/s M-PPM
BER	**10^{-7}**	**10^{-5}**	N/A	10^{-9}	N/A	10^{-3}	10^{-3}	10^{-3}	10^{-3}
FoM (Energy/Bit)	**11.2nJ/b**	**3.6nJ/b**	N/A	0.7nJ/b	N/A	6.8µJ/b	128.3nJ/b	19.9nJ/b	N/A
RX Sensitivity/RX P_{DC} (dBm/mW)	**-89/31.1**		N/A	-60/866	-64/68	-54/0.036	-93/1.85	-77/0.306	N/A
Technology	**45nm CMOS SOI**		130nm BiCMOS	130nm BiCMOS	32nm CMOS SOI	180nm CMOS	180nm CMOS	180nm BiCMOS	65nm CMOS

* TX peak P_{DC} assumes OOK/ASK modulations. RX peak P_{DC} includes the on-chip TDC DC power of 0.75mW.

† Defined as Sensitivity = -174dBm/Hz + 10logBW + NF with BW = 8GHz.

Designs in [32] [33] [34] are reported Si-based 300GHz TRXs. Designs in [11] [12] [13] [22] are reported low-power radios at MHz, GHz, and mm-Wave frequencies.

CHAPTER 5. A MULTI-PHASE SUB-HARMONIC INJECTION LOCKING TECHNIQUE FOR BANDWIDTH EXTENSION IN SILICON-BASED TERAHERTZ SIGNAL GENERATION

This chapter presents a multi-phase injection locking (IL) technique and its application in the locking range extension in multi-phase injection locking oscillators (ILOs) for Terahertz (THz) signal generation. The proposed technique can significantly increase the frequency locking range of a multi-phase injection locking oscillator compared to the conventional single-phase injection locking scheme. Based on the multi-phase IL technique and sub-harmonic ILOs, an "active frequency multiplier chain" architecture and a multi-ring system layout topology are also proposed to achieve scalable THz signal generation. As proof of concept, a cascaded 3-stage 3-phase 2^{nd}-order sub-harmonic ILO chain is implemented in the IBM 9HP SiGe BiCMOS process. The design achieves a maximum output power of -16.6dBm at 498GHz, a phase noise of -87dBc/ Hz at 1MHz offset, and a total 5.1% frequency tuning range from 485.1GHz to 510.7GHz, which is the largest frequency tuning range among all the reported silicon-based THz oscillator sources in the 0.5THz band.

5.1 Introduction

THz range, from 0.3THz to 3THz in the electromagnetic spectrum, has recently stimulated an increasing research interest with their unique applications, such as molecular spectroscopy, THz imaging, radar, and high-speed communication [99]–[101]. One of the major technology roadblocks of applying THz technologies lies in the lack of low-cost and

compact THz sources. Most existing THz setups are based on discrete compound devices, bulky optics or quantum cascade lasers. Although these sources may support large output power at THz [102] [103], their low integration level, high-cost, and need for dedicated setups often limit their usage only in high-end research labs.

On the other hand, the continuous device scaling in silicon technologies (CMOS or SiGe BiCMOS) has shown tremendous promise to realize self-contained THz systems with low cost and compact form-factor [108]–[123]. However, there are several fundamental challenges for silicon technologies to generate large output power at THz range. First of all, according to the Johnson Limit [124], the product of the unity gain cutoff frequency f_T and the breakdown voltage V_m of a transistor is approximately a constant for a given semiconductor material, as

$$V_m \cdot f_T = \frac{E_m v_s}{2\pi}, \tag{5.1}$$

where E_m is the maximum electric field and v_s is the electron saturation velocity. As a result, although advanced silicon process nodes can provide higher f_T/f_{max}, the breakdown voltage also decreases, reducing the maximum allowed voltage swing and thus maximum output power delivered to the load. Secondly, the loss of the passive structures in standard silicon technologies does not decrease with device down-scaling either. This is because the thickness of top metal layers remains almost the same in scaled process nodes, which results in similar passive efficiency. The low-resistivity silicon substrate is another major loss factor for inductors, transformers and on-chip antennas in bulk silicon processes, which again, does not improve in advanced process nodes except for special processes,

such as Silicon-on-Insulator (SOI) or Silicon-on-Sapphire (SoS). Vertical interconnects are getting more attractive at THz frequencies, but at the cost of post-processing and integration complexity. Therefore, there is an increasing need for design innovations on the circuit topologies and system architectures to improve the output power capability of silicon devices in the THz frequency range.

Besides sufficient output power, a broad bandwidth is equally important in many THz applications. For example, in an FMCW imaging radar, the range resolution of the radar is inversely proportional to its bandwidth [125]. Therefore, a higher range resolution can be achieved by increasing the system bandwidth. A large bandwidth is also critical in hyperspectral imaging systems, which measures the spectrum information of each pixel during the imaging to identify objects, characterize materials, and detect chemical processes [135] [136]. In addition, THz spectroscopy also prefers a large bandwidth to cover sufficient resonant peaks in the absorption spectrum [99] Therefore, it is highly desirable for silicon-based THz sources to achieve both sufficient output power and bandwidth.

Figure 5.1 summarizes recently reported power generation designs in silicon. Below 150GHz, most designs are based on power amplifiers (PAs). This is because silicon transistors can provide sufficient power gain in this frequency range, which allows the implementation of PAs with both high output power and efficiency. Around 100GHz, power generation based on fundamental oscillators starts to become a viable design choice. These designs leverage the nature of oscillation to compensate the reduced transistor gain at these frequencies. However, the oscillation frequency of a fundamental oscillator is limited by the transistor f_{max}. Moreover, varactors commonly exhibit low quality factors

(Q) in this frequency range, leading to a direct trade-off between frequency tuning range and output power. Above 150GHz, the intrinsic gain of silicon transistors starts to become inefficient to support power amplification. Therefore, passive frequency multipliers based on nonlinear passive devices, e.g., diodes and varators, become popular design choices to generate harmonic signals from mm-wave pumping signals. Passive multipliers often offer broad bandwidths and consume low DC power. However, they also present substantial conversion loss during the passive harmonic generation, and therefore require inter-stage amplifiers to boost the signal level. The designs of these inter-stage amplifiers may become challenging to meet the high pumping signal power demands required by high-frequency passive multipliers. Another popular approach is to extract the harmonic signals from mm-wave oscillators. For example, the N-push oscillator (multi-phase oscillator) can naturally enable N^{th} harmonic extraction at its common node, while the fundamental tone and the 2^{nd} through $(N\text{-}1)^{th}$ order harmonics, are cancelled. In addition, there is no need for any high-power driving stages. Therefore, the multi-phase oscillator has been a widely adopted technique to achieve THz power generation beyond f_{max} in silicon, although its frequency tuning range is often limited compared to passive multipliers.

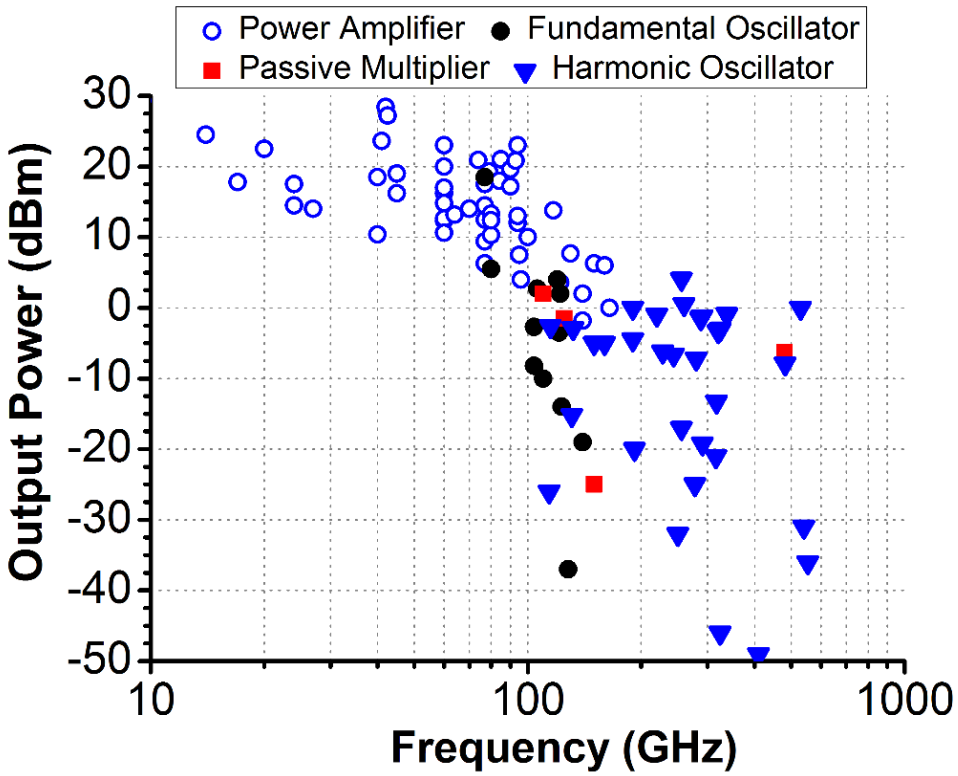

Figure 5.1 – Recently reported power generation designs in silicon technologies (CMOS and SiGe BiCMOS).

In this chapter, a multi-phase injection locking (IL) technique is proposed, which can lock the *N*-push oscillator for coherent THz signal generation with both locking bandwidth extension and signal balancing for efficient harmonic extraction. Then, by employing multi-phase IL in sub-harmonic injection locking oscillators (ILOs), I also demonstrate an "active frequency multiplier" for frequency multiplication and signal restoration/amplification without any amplifiers. This enables a cascadable system architecture with several multi-phase sub-harmonic ILOs implemented in a chain to generate the THz signal from a reference source at a considerably lower frequency, e.g., tens of GHz. Such a low-frequency signal can be readily derived from a high-quality on-chip synthesizer for high spectral purity. Moreover, this cascadable topology opens the door for a scalable THz signal generation array, where each element can be locked to the

common reference signal, and the THz signals from the array elements can be coherently combined to increase the output power. As proof of principle, a 3-stage 3-phase 2nd-order sub-harmonic ILO chain is demonstrated in this thesis [108]–[110]. It achieves a system tuning range of 5.1% (from 485.1GHz to 510.7GHz) with a phase noise of -87dBc/Hz at 1MHz offset, which is the largest frequency tuning range and best phase noise among all reported silicon-based THz oscillator sources in the 0.5THz band. Its maximum output power is -16.6dBm at 498GHz, and it achieves more than -20dBm across the system frequency tuning range.

This chapter is organized as follows. Section 5.2 presents the proposed multi-phase IL technique and demonstrates its benefits compared to the conventional single-phase IL approach. The scalable "active frequency multiplier" chain system topology and the design details of the 500GHz power generation system are presented in Section 5.3. The measurement results are shown in Section 5.4. Section 5.5 concludes this chapter with a performance comparison table.

5.2 Multi-Phase Injection Locking Technique

The multi-phase IL scheme was previously reported in the designs of an RF frequency divider [126] and a THz frequency divider [120]. We leverage the bandwidth extension nature of the multi-phase ILO to the THz signal generation. The following discussions will focus on an N-push oscillator operation, its harmonic extraction for THz signal generation, and its synchronization with multi-phase IL signals.

5.2.1 N-Push (Multi-Phase) LC Ring Oscillator

As an example, a 3-phase *LC* ring oscillator (120°-mode) is shown in Figure 5.2(a). At the free-running frequency, the relative phases of the voltages V_1, V_2 and V_3 are 0°, 120° and 240° in the phasor analysis. Assume the transistors have negligible parasitic feed-through, the collector current (e.g., I_{osc1}) and the base voltage (e.g., V_1) of each transistor should be out of phase (180°). Thus, the *LC* tank provides -60° phase shift as its tank impedance to keep the 120° phase offset between the voltages of adjacent stages, e.g., V_1 and V_2 [Figure 5.2(b)]. Assuming a constant quality factor Q around the natural resonance frequency ω_0 of the *LC* tank, the tank impedance is

$$Z(j\omega) = \frac{1}{\frac{1}{R} + \frac{1}{j\omega L} + j\omega C} = \frac{j\omega L}{\frac{j\omega L}{R} + (1 - \omega^2 LC)} = \frac{j\omega L}{\frac{j}{Q} + (1 - \frac{\omega^2}{\omega_0^2})}, \tag{5.2}$$

where R, L, and C are the parallel resistance, inductance, and capacitance of the tank. The quality factor and the resonant frequency are defined as

$$Q = \frac{R}{\omega L} \text{ and } \omega_0^2 = \frac{1}{LC}. \tag{5.3}$$

The phase of the tank impedance φ, i.e., the phase difference between tank current and voltage, is

$$\varphi = \frac{\pi}{2} - \arctan\left(\frac{1}{Q} \cdot \frac{\omega_0^2}{\omega_0^2 - \omega^2}\right) \text{for } \omega < \omega_0 \text{ , and} \tag{5.4}$$

$$\varphi = -\frac{\pi}{2} + \arctan\left(\frac{1}{Q} \cdot \frac{\omega_0^2}{\omega^2 - \omega_0^2}\right) \text{for } \omega > \omega_0 \,. \tag{5.5}$$

Note that with the definitions in (5.4) and (5.5), $0 < \varphi < \pi/2$ for $\omega < \omega_0$, and $-\pi/2 < \varphi < 0$ for $\omega > \omega_0$. Therefore, if the 3-phase ring oscillator oscillates in the 120°-mode, the oscillation frequency ω_{osc} should be higher than the resonant frequency ω_0 to provide the required -60° phase shift, as

$$\omega_{\text{osc}} = \sqrt{\frac{\sqrt{3}}{Q} + 1} \cdot \omega_0 \,. \tag{5.6}$$

The voltage phasors V_1, V_2 and V_3 at f_0, $2f_0$, and $3f_0$ are shown in Figure 5.2(c). Assume there is no mismatch among all 3 stages, the 3rd harmonic signals from each stage are in-phase with the same amplitude and can be added constructively at the common node V_{out}. At the same time, all the harmonics which are not multiples of 3, e.g., f_0, $2f_0$, and $4f_0$, are naturally cancelled at V_{out} [111]. Therefore, this architecture allows the 3rd harmonic extraction for THz signal generation.

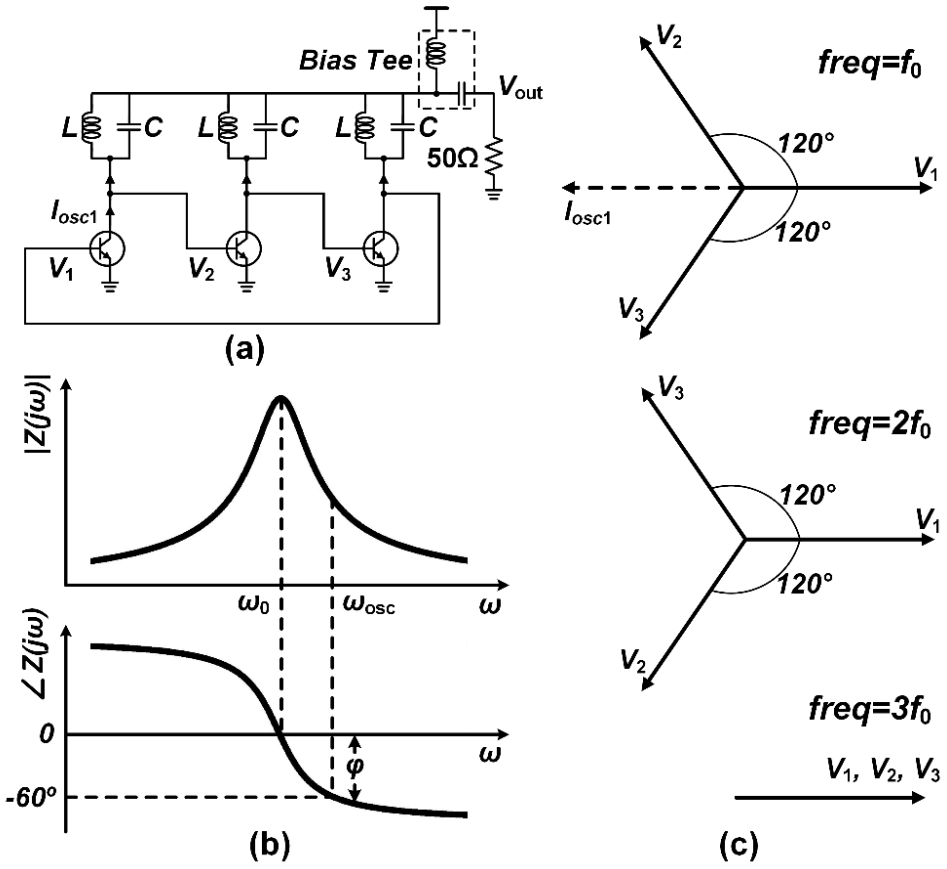

Figure 5.2 – (a) A 3-phase *LC* ring oscillator in the 120°-mode. (b) The amplitude and phase of the *LC* tank impedance. (c) Voltage phasors at f_0, $2f_0$, and $3f_0$.

5.2.2 Multi-Phase Injection Locking Scheme

The simplified schematics of the single-phase and multi-phase IL schemes in a ring oscillator are shown in Figure 5.3. The conventional single-phase IL scheme feeds all the injection power into a single node. In contrast, in the proposed multi-phase IL scheme, the total injection power is split into *N*-ways and applied to each stage with the proper phase shifts to match the desired oscillation mode. To make a fair comparison on the resulting frequency locking range, the same total injection power is applied for the two schemes. Thus, the amplitude of the single-phase injection current is $\sqrt{N}$ larger than that in the multi-phase case, where *N* is the number of stages in the *N*-push oscillator.

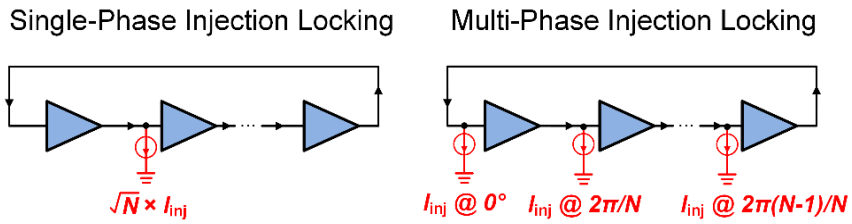

Figure 5.3 – Single-phase vs. multi-phase injection locking scheme.

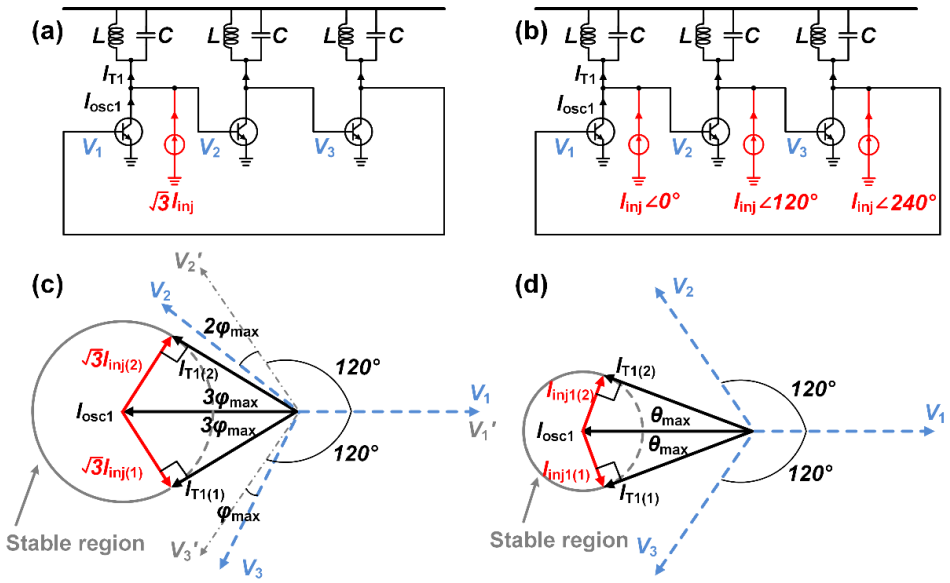

Figure 5.4 – (a) A 3-phase *LC* ring oscillator with the single-phase injection locking (IL) scheme. (b) A 3-phase *LC* ring oscillator with the three-phase IL scheme. (c) The phasor diagram denoting the maximum phase shift in the single-phase IL scheme. (d) The phasor diagram denoting the maximum phase shift in the three-phase IL scheme.

The multi-phase IL scheme is analyzed first by using a 3-phase *LC* ring oscillator as an example [Figure 5.4(b)]. The 3-phase IL scheme assumes that the 3 injection currents at ω_{inj} with 0°, 120°, and 240° phases are applied at the 3 transistor collectors. These injection currents are able to lock the oscillator from free-running frequency ω_{osc} to the injection frequency ω_{inj}. Due to the symmetry, the node voltages V_1, V_2, and V_3 automatically preserve the balanced amplitude and 120° phase difference [Figure 5.4(d)]. Taking the first stage of the oscillator as an example, the *LC* tank current I_{T1} is a vector sum of the collector current I_{osc1} and the injection current I_{inj1}. The phase difference

between the tank current I_{T1} and the tank voltage V_2 is due to the tank impedance function (5.2) with $\omega=\omega_{inj}$. Therefore, the frequency locking range of the oscillator can be determined by locating the maximum and minimum phase difference between I_{T1} and V_2 as a function of the I_{inj1}, whose possible vector values form a circle centered at I_{osc1}. On the phasor vector plot [Figure 5.4(d)], the maximum phase difference between I_{osc1} and I_{T1} can be found as,

$$\theta_{\max} = \arcsin\left(\frac{I_{\text{inj}}}{I_{\text{osc}}}\right), \tag{5.7}$$

$$-\left(\frac{\pi}{3} + \theta_{\max}\right) = -\frac{\pi}{2} + \arctan\left(\frac{1}{Q}\cdot\frac{\omega_0^2}{\omega_{\text{h}}^2 - \omega_0^2}\right), \text{and} \tag{5.8}$$

$$-\left(\frac{\pi}{3} - \theta_{\max}\right) = -\frac{\pi}{2} + \arctan\left(\frac{1}{Q}\cdot\frac{\omega_0^2}{\omega_{\text{l}}^2 - \omega_0^2}\right), \tag{5.9}$$

where θ_{max} represents the maximum phase difference between I_{osc1} and I_{T1}; ω_h is the higher frequency locking boundary; ω_l is the lower frequency locking boundary. From (5.8) and (5.9), the frequency locking boundaries can be determined as

$$\omega_{\text{h}} = \sqrt{\omega_0^2 + \frac{\omega_0^2}{Q\cdot\tan\left(\frac{\pi}{6} - \theta_{\max}\right)}} \text{ and}$$
$$\omega_{\text{l}} = \sqrt{\omega_0^2 + \frac{\omega_0^2}{Q\cdot\tan\left(\frac{\pi}{6} + \theta_{\max}\right)}}. \tag{5.10}$$

Therefore, the final normalized frequency locking range can be derived as

$$\frac{\omega_{\mathrm{h}}-\omega_{\mathrm{l}}}{\omega_{\mathrm{osc}}}=\frac{\sqrt{Q+\frac{1}{\tan\left(\frac{\pi}{6}-\theta_{\max}\right)}}-\sqrt{Q+\frac{1}{\tan\left(\frac{\pi}{6}+\theta_{\max}\right)}}}{\sqrt{Q+\sqrt{3}}}. \tag{5.11}$$

Next, the voltage and current phasor relationship for the single-phase IL scheme is analyzed [Figure 5.4(a) and 5.4(c)]. In this case, the IL current $\sqrt{3}I_{\mathrm{inj}}$ acts only at a single node, resulting in two issues particularly relevant for harmonic-based THz signal generation. First, the single injection node now needs to provide all the additional phase shift between I_{osc} and I_{T} (previously distributed equally among all the 3 nodes in the three-phsae IL scheme) to ensure locking. Assume the maximum phase difference between I_{osc1} and I_{T1} is $3\varphi_{\max}$ with $\varphi_{\max}$ as

$$\varphi_{\max}=\frac{1}{3}\arcsin\left(\frac{\sqrt{3}I_{\mathrm{inj}}}{I_{\mathrm{osc}}}\right). \tag{5.12}$$

Thus, the minimum and maximum phase differences between I_{T1} and V_2 equal $-(\pi/3-\varphi_{\max})$ and $-(\pi/3+\varphi_{\max})$, respectively, and the locking range can be derived using (5.8)–(5.11).

To compare the frequency locking range of the three-phase IL scheme and the single-phase IL scheme, one can directly compare $\theta_{\max}$ and $\varphi_{\max}$, which are the maximum additional phases provided by the *LC* tank for the three-phase IL/single-phase IL scheme (Figure 5.4). Take the difference between $\theta_{\max}$ and $\varphi_{\max}$ as

$$\theta_{max} - \varphi_{max} = \arcsin\left(\frac{I_{inj}}{I_{osc}}\right) - \frac{1}{3}\arcsin\left(\frac{\sqrt{3}I_{inj}}{I_{osc}}\right). \tag{5.13}$$

The first derivative of (5.13) can be calculated as

$$\frac{d(\theta_{max} - \varphi_{max})}{d\left(\frac{I_{inj}}{I_{osc}}\right)} = \frac{1}{\sqrt{1 - \left(\frac{I_{inj}}{I_{osc}}\right)^2}} - \frac{1}{\sqrt{3 - 9\left(\frac{I_{inj}}{I_{osc}}\right)^2}}. \tag{5.14}$$

Note that the phase provided by an *LC* tank should be between -π/2 and π/2. In addition, the phase of the *LC* tank equals π/3 at the free-running frequency (in the 120º-mode). Therefore, an additional phase shift of the tank due to IL is within π/6, so I_{inj}/I_{osc} should be smaller than 0.5 to ensure $\theta_{max} < \pi/6$ based on (5.7).

From (5.13) one can get $\theta_{max} = \varphi_{max}$ only for $I_{inj}/I_{osc}=0$. Furthermore, from (5.14) one can get

$$\frac{d(\theta_{max} - \varphi_{max})}{d\left(\frac{I_{inj}}{I_{osc}}\right)} > 0 \text{ for } \frac{I_{inj}}{I_{osc}} < 0.5\,, \tag{5.15}$$

meaning that $\theta_{max} > \varphi_{max}$ always holds for $I_{inj}/I_{osc} < 0.5$.

Therefore, the three-phase IL scheme provides a larger additional phase shift of the *LC* tank compared to the single-phase IL scheme, meaning that the three-phase IL scheme can achieve a larger frequency tuning range with the same total injection power. The analysis can be generalized to the *N*-phase IL scheme to show that it out-performs its single-phase IL counterpart.

The frequency locking ranges for these two schemes at different tank Q-factors are computed based on (5.7), (5.11) and (5.12), and are plotted in Figure 5.5(a). For a given total IL power, the 3-phase IL scheme always offers a larger frequency locking range. Circuit simulations also confirm the superior locking range of the multi-phase IL scheme [Figure 5.5(b)] based on the schematics shown in Figure 5.4. In this basic simulation demonstration, the injection currents are provided by ideal current sources and no device parasitics are included for simplicity. The HBTs are based on the IBM 9HP design kit model with 5μm×100nm as their emitter size and a supply voltage of 1.5V.

The other issue in the single-phase IL scheme is that the node voltages V_1, V_2, and V_3 will deviate from the desired symmetry. For example, if the IL current $\sqrt{3}I_{\text{inj}(1)}$ adds extra phase 3φ in the loop, the original voltage phasors V_2' and V_3' will rotate to V_2 and V_3, respectively. As a result, the phase difference between V_3 and V_1 (or V_2 and V_3) equals $120°–\varphi$ where the phase difference between V_1 and V_2 is $120°+2\varphi$ [Figure 5.4(c)]. Note that this phase imbalance will be 2 times larger for the 2nd harmonic and 3 times larger for the 3rd harmonic signals. It compromises the fundamental and 2nd harmonic suppression and more importantly degrades the in-phase power combining and extraction of the 3rd harmonic signals at the common node. The simulation results from Figure 5.5(b) also show that the simulated 3rd harmonic output power for three-phase IL is always higher than its single-phase IL counterpart.

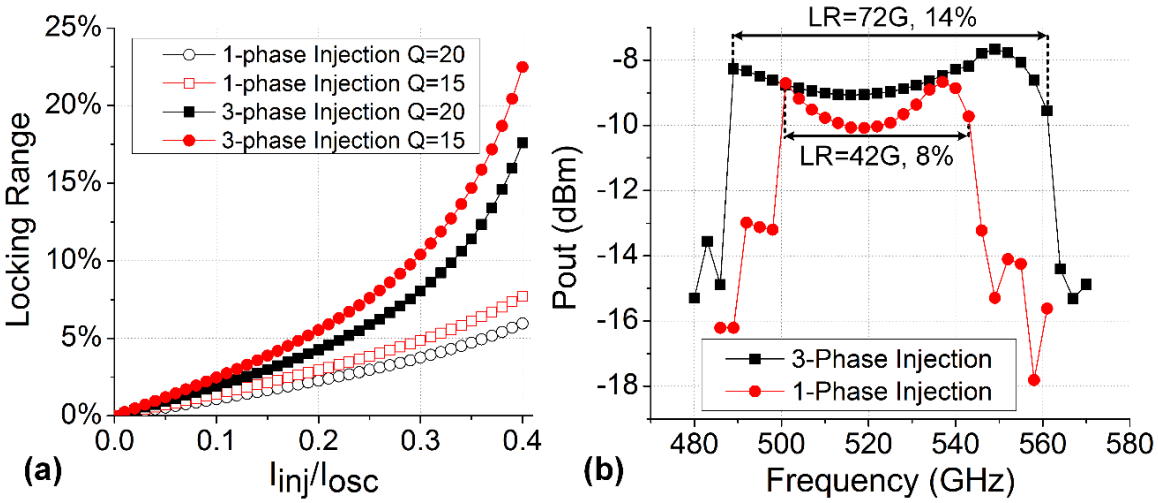

Figure 5.5 – (a) Theoretically calculated locking ranges for the multi-phase and single-phase IL schemes on a 3-phase oscillator (Figure 4a and Figure 4b) at different tank *Q* (quality factor). (b) Schematic simulation of the locking range of a 3-phase 175GHz oscillator (I_{inj}/I_{osc}=0.33) with current source injection for producing its 3rd harmonic signal at 525GHz.

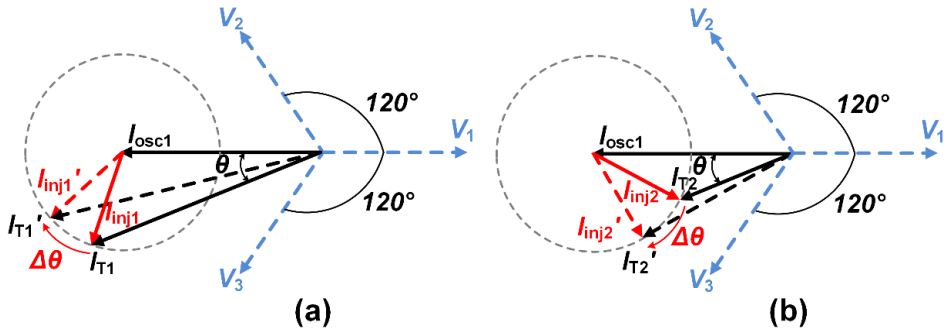

Figure 5.6 – Perturbation analysis for two possible modes. (a) The stable mode. (b) The unstable mode.

In addition, for frequencies within this locking range, there are two possible phase solutions (Figure 5.6). The perturbation analysis [127] can be utilized to show that only the mode in Figure 5.6(a) is stable. A graphical proof can be applied on the phasor diagram to demonstrate the mode stability. Assume ω_{inj} is larger than ω_0 for the mode in Figure 5.6(a). If the phase of V_1 experiences a small perturbation by a positive angle $\Delta\theta$, the phase of I_{inj1} lags by the same angle $\Delta\theta$, as shown in Figure 5.6(a). Therefore, the phase difference

between I_{T1} and I_{osc1} will decrease and result in a frequency decrease of the oscillator. This counteracts with the phase advance of V_1, meaning that the mode in Figure 5.6(a) is stable. Similarly, for the mode in Figure 5.6(b), with a small perturbation by a positive angle $\Delta\theta$ in V_1, the oscillation frequency will increase, indicating the instability of this mode. To summarize this perturbation analysis, the stable regions are denoted in Figure 5.4(c) and Figure 5.4(d).

5.3 A Scalable and Cascadable Multi-Phase Sub-Harmonic Injection Locking Architecture for THz Signal Generation

Based on the multi-phase IL technique, a scalable and cascadable "active frequency multiplier" architecture is proposed to achieve THz generation from a mm-wave tone. The system architecture and the detailed design considerations are presented below.

5.3.1 System Architecture

The multi-phase IL is combined with the sub-harmonic ILOs to realize an "active frequency multiplier" (Figure 5.7). First, the input of the system can be generated at f_0 by a mm-wave or RF signal source, e.g., a PLL or a free-running VCO. Then, the N_1^{th} harmonic signals of the input and extracted and injected to an oscillator operating at $N_1 \times f_0$. The ILO ensures the frequency/phase synchronization with the input tone at f_0. More importantly, it restores the signal amplitude at $N_1 \times f_0$ after the frequency multiplication to compensate the conversion loss in the harmonic generation. Next, the N_2^{th} harmonic signals from the first ILO and are injected to the next ILO at $N_1 \times N_2 \times f_0$ frequency. By cascading these sub-harmonic ILOs, an "active frequency multiplier" chain is created. Finally, the harmonic signal from the last stage ILO can be extracted as the desired THz output signal.

Note that the system can be conveniently achieved if all the ILOs are implemented as multi-phase oscillators which provide bandwidth extension and signal balancing simultaneously.

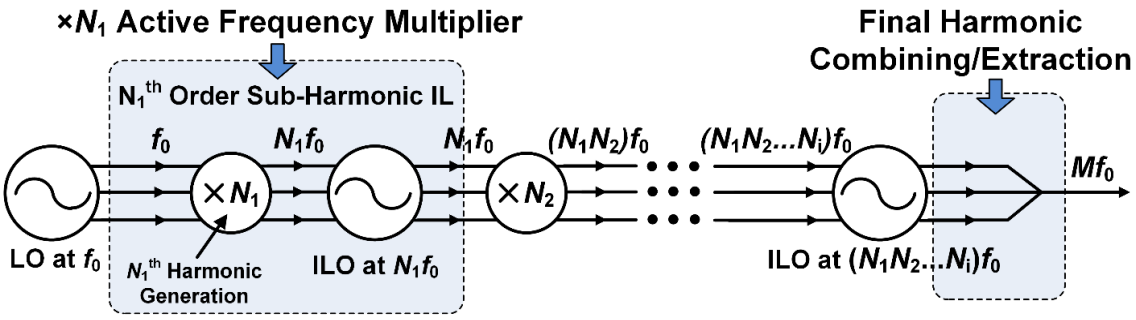

Figure 5.7 – The proposed system architecture as an "active frequency multiplier" chain.

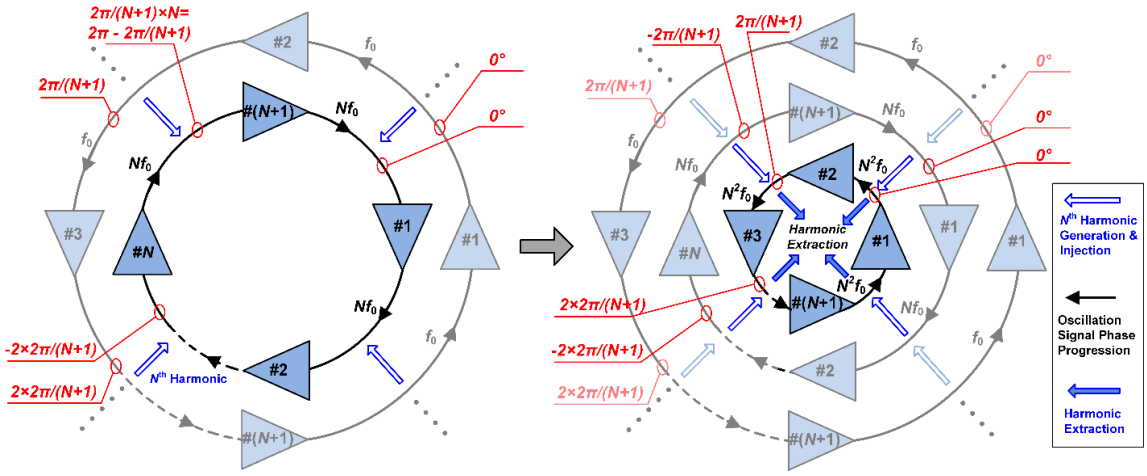

Figure 5.8 – The proposed ring style system layout scheme.

Moreover, the proposed "active frequency multiplier" chain can be realized in a multi-ring topology if the sub-harmonic index and the multi-phase ILO stage number are co-prime. A special case for the N^{th} sub-harmonic IL and (N+1)-phase ILO is shown in Figure 5.8. Assume that the outermost ring is an (N+1)-stage ILO with its phase progression in the counter-clockwise direction at f_0 and the phase difference between each adjacent stage is $2\pi/(N+1)$. Thus, the phases at each stage are 0, $2\pi/(N+1)$, and $4\pi/(N+1)$, etc. If the N^{th} harmonic signals from each stage of this ILO are used to injection-lock the

2^{nd} outermost ring ILO, the phases of these N^{th} harmonic signals are 0, $-2\pi/(N+1)$, and $-4\pi/(N+1)$, etc. Using these harmonic signals for locking, the 2^{nd} outermost ring thus should oscillate with its phase progression in the clockwise direction, i.e., in the reversed direction compared to the outermost ring. Similarly, if the N^{th} harmonics of the $(N+1)$ signals from the 2^{nd} outermost ring ILO are used to lock the 3^{rd} ring ILO, this will result in a counter-clockwise oscillation mode for the 3^{rd} ring ILO. The signal frequency is gradually multiplied up from the outer rings to the inner rings, and all the rings can be mutually locked. Finally, the innermost ring ILO oscillates at the highest frequency, and its harmonic signal can be extracted as the desired THz output signal. This proposed ring style layout scheme provides the desired phase progression and significantly simplifies the high-frequency signal routing, which are highly critical in the THz designs. Moreover, by employing more outer rings, the input frequency of the system can be further reduced.

This system architecture can also be scaled to an array where each element can be locked to a common reference at a considerably lower frequency, e.g., tens of GHz, by using the proposed sub-harmonic IL chain. Therefore, THz signals from the array elements can be coherently combined to further increase the output power. Note that the multi-phase outermost ring oscillator can be potentially included into an on-chip PLL. For example, one output from the multi-phase outermost ring can be connected to the frequency divider in the PLL, while the other outputs are connected to dummy loads to keep the balancing. Using this approach, the outermost ring oscillator can be locked to a MHz crystal reference signal, which will further facilitate the reference signal distribution among the array elements.

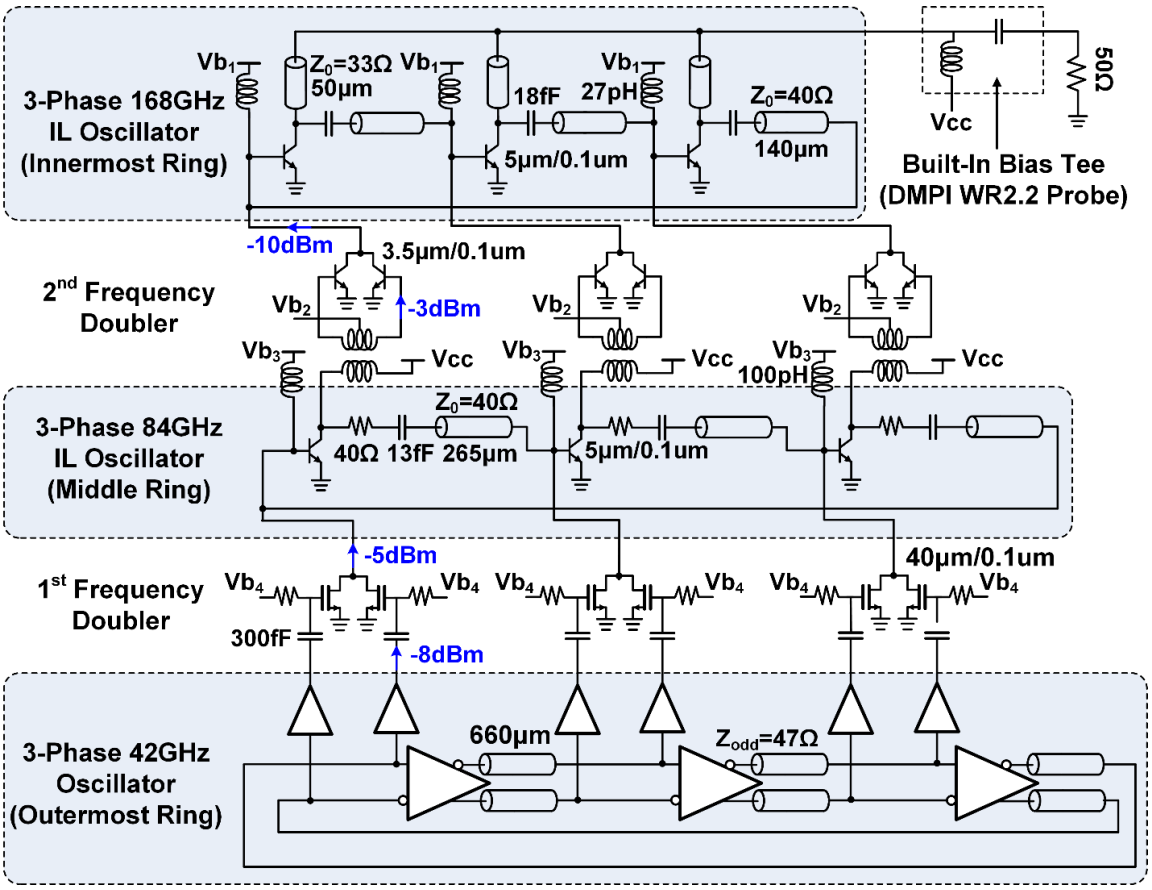

Figure 5.9 – Circuit schematic of the THz signal generation system.

As proof of concept, a cascaded 3-stage 3-phase 2nd-order sub-harmonic ILO chain for 500GHz signal generation is implemented (Figure 5.9). The design details are shown below.

5.3.2 Process Technology

The THz signal generation circuit is implemented in the IBM 9HP SiGe BiCMOS process. It is a 90-nm process node which features high-speed SiGe HBTs with a maximum f_T/f_{max} of 300/350GHz. The BV_{CEO} of the high-speed HBT is 1.5V. This technology uses HiCUM model for the HBT devices. The design kit also provides MOSFETs with a drawn gate length of 100nm.

5.3.3 The 3-Phase 168GHz Oscillator (Innermost Ring ILO)

The innermost ring, i.e., the final stage of the system, is a 3-phase 168GHz ILO (120°-mode). The equivalent circuit for a single stage is shown in Figure 5.10. To generate the maximum output power for a transistor at a given fundamental frequency, there exists optimum conditions for the gain (A_{opt}) and phase difference (φ_{opt}) between the input and output of the transistor [111]. These optimum conditions are given as

$$A_{\text{opt}} = \sqrt{\frac{Re\{Y_{11}\}}{Re\{Y_{22}\}}}\,, \tag{5.16}$$

$$\varphi_{\text{opt}} = (2k+1)\pi - \angle(Y_{12} + Y_{21}^{*})\,. \tag{5.17}$$

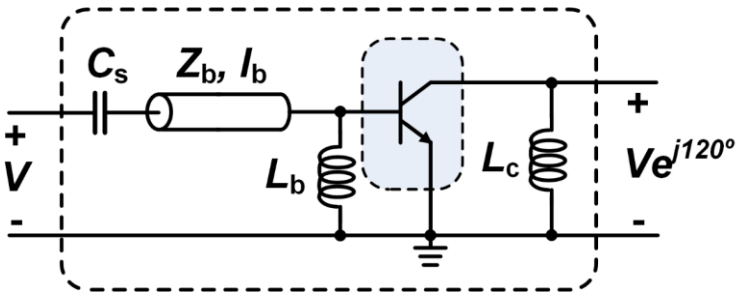

Figure 5.10 – Equivalent circuit for a single stage ILO at fundamental frequency f_0.

Figure 5.11 shows the simulated A_{opt} and φ_{opt} for a stand-alone HBT device (emitter size = 5μm×100nm). At 168GHz, the simulated A_{opt} is 2 and φ_{opt} is 113°. Since the simulated φ_{opt} is close to 120°, a 3-phase *LC* ring oscillator topology with a +120° phase progression becomes a natural choice. Improving the oscillator voltage swing at the fundamental frequency also makes the device more nonlinear and facilitates the 3rd harmonic current generation.

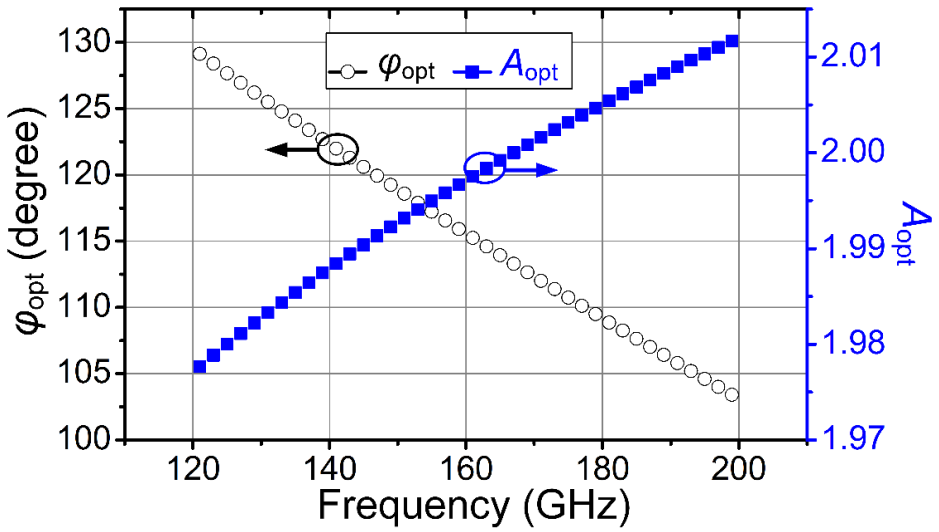

Figure 5.11 – The optimum amplitude and phase conditions for a HBT with size of 5μm×100nm.

Shunt inductor L_b is added to resonate out the parasitic base capacitance of the HBT as well as provide DC bias for the base. L_b is realized by a short T-Line as 27pH at 168GHz. Series capacitor C_s of 18fF is used to block the DC between the adjacent stages. The T-line, with a characteristic impedance of Z_b=40Ω and length of l_b=140μm, together with C_s further helps the HBT to meet both optimum gain and phase difference conditions in (5.16) and (5.17).

At $3f_0$, the equivalent schematic of one stage is shown in Figure 5.12(a). The nonlinearity of the HBT generates the 3rd harmonic current I_{3f0} at the collector. The currents (I_{3f0}) from each of the 3 branches are all in phase, each stage thus has an equivalent load of 150Ω. Moreover, in this equivalent circuit, the node connected to the collector of the previous stage (to the left of C_s) can now be directly connected to the collector of the current stage to simplify the analysis with the loading effects. In order to deliver more power at $3f_0$ to the load, the impedance Z_1 should be boosted, so that more $3f_0$ harmonic current can sink into the load. As shown in Figure 5.12(b), after the impedance transformation of the T-line

and C_s, the low base impedance can be increased by a factor of 3.5 from 8.8Ω to 31Ω, as expressed by

$$Z_1 = \frac{1}{j\omega C_s} + Z_b \cdot \frac{Z_{base} + jZ_b \tan(\beta l_b)}{Z_b + jZ_{base} \tan(\beta l_b)}. \quad (5.18)$$

Based on the harmonic balance simulations, the base voltage swing at $3f_0$ is 13dB lower than the collector voltage swing. Although a shorter T-line will further increase Z_1 at $3f_0$ with better 3rd harmonic blocking, there exists a practical trade-off, since this T-line length is limited by the size of the innermost ring ILO to accommodate the output GSG pads and output combining network.

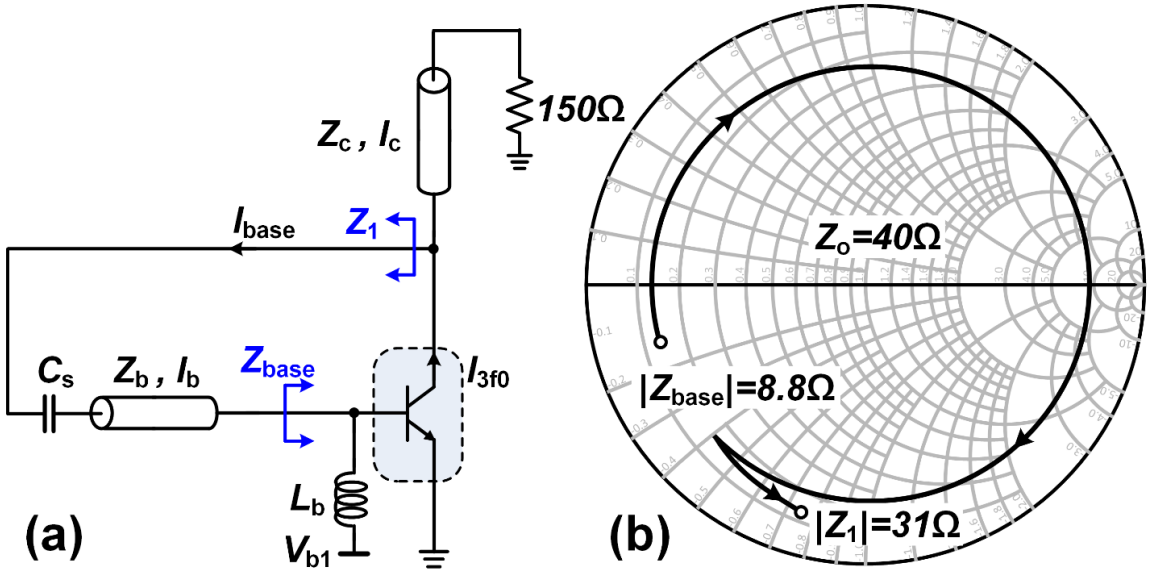

Figure 5.12 – (a) Equivalent circuit for a single stage ILO at $3f_0$. (b) The low Z_{base} is transformed to a higher impedance at $3f_0$ through T-line and C_s.

Short T-lines serve as the peaking inductors at the collectors as well as the 3rd harmonic extraction network. Since it is critical to maintain the symmetry of the layout and account for any parasitic coupling, all T-lines, connections and output GSG pads are co-

designed using a 3D EM simulator HFSS [Figure 5.13(a)]. The simulated transient oscillation waveforms based on the actual layout and the 3D EM modeling are shown in Figure 5.13(b). Despite all the non-ideal effects of the practical layouts and routings, the oscillation waveforms still preserve good symmetry and balancing. The simulated frequency locking range of the innermost ring is shown in Figure 5.14(a), which includes the loading of the 2nd-stage frequency doublers and assumes a total injection power of 4.8dBm at 84GHz. A simulated locking range of 6.8% and a maximum output power of -13dBm are achieved. Compared with Figure 5.5(b), the frequency locking range is reduced and the peak output power also decreases because of the loading effect from the IL circuits, the limited available injection power from the previous stage, device layout parasitics, and the degraded routing symmetry in the EM structure. Figure 14b shows a typical output spectrum in this full extracted simulation with the fundamental, 2nd, 3rd, 4th, 5th, and 6th order harmonics. A P_{out} of -13dBm is achieved at the 3rd order harmonic. The fundamental leakage is 13dB lower than the 481.2GHz output signal while the 2nd harmonic is suppressed by 29dB. Without applying injection power, the simulated phase noise at the fundamental frequency is -85.2dBc/Hz at 1MHz offset and the simulated phase noise of the 3rd harmonic output signal is -75.7dBc/Hz at 1MHz offset.

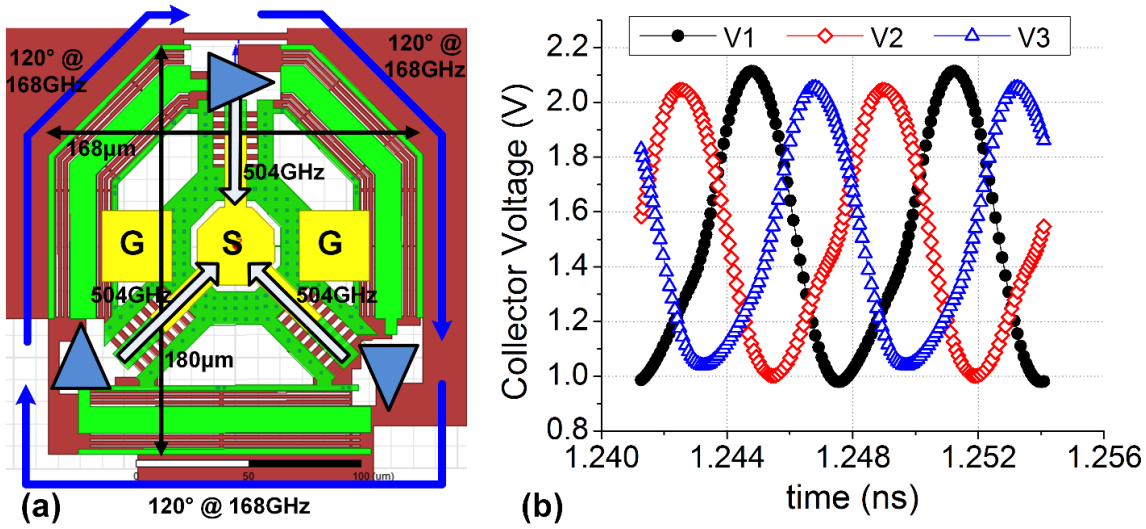

Figure 5.13 – (a) The passive structure of the 3-phase 168GHz oscillator. (b) Transient simulation of the 3-phase 168GHz oscillation waveforms with the layout extraction and the 3D EM modeling.

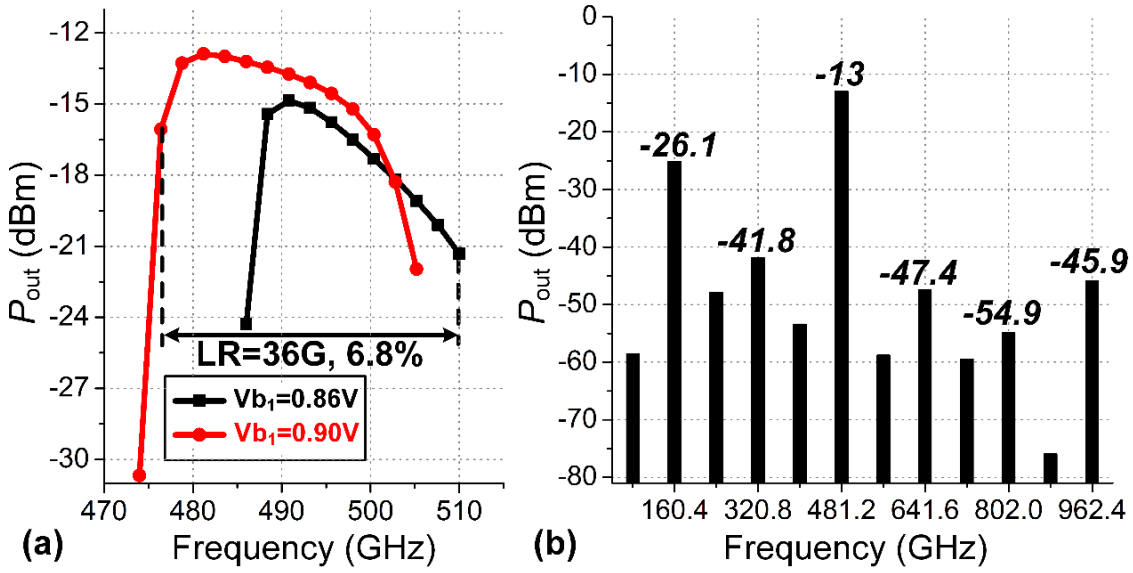

Figure 5.14 – (a) Simulated locking range of the innermost ring ILO. (b) Simulated output spectrum with the fundamental and the 2nd, 3rd, 4th, 5th, and 6th order harmonics. A P_{out} of -13dBm is achieved at the 3rd order harmonic.

5.3.4 The 3-Phase 84GHz Oscillator (Middle Ring ILO)

Similar to the innermost ring ILO, the middle ring is a 3-phase *LC* ring oscillator at 84GHz, but oscillating in the 240°-mode. In order to ensure that the locking range of the

middle ring can cover the locking range of the innermost ring under PVT variations, series resistors of 40Ω are added at each stage to boost the locking range by slightly sacrificing the loop gain (Figure 5.9). The simulated frequency locking range of the middle ring is 8.6%. A passive transformer-based balun is employed at each output to generate differential signals, which are then fed to a frequency doubler (push-push pair) to generate the injection currents at 168GHz for the innermost ring ILO.

The passive balun adopts a compact transformer-based design with its 3D EM model shown in the Figure 5.15(a). Transformer-based baluns are widely used in RF applications since they can provide well-balanced outputs with a broad bandwidth, and achieve impedance transformation within a single inductor footprint [12]. However, a balancing issue may arise at high frequency because of the distributed capacitive coupling between the primary and secondary coils. In a transformer-based balun, the primary coil is driven in a single-ended fashion with one terminal connected to the AC ground. Therefore, from the capacitive coupling perspective, the primary coil couples a strong signal to the secondary coil at its un-grounded terminal (i.e., input feed), but it only couples a weak signal at its grounded terminal. This is the fundamental reason of the unbalanced behavior of a transformer-based balun at high-frequency. Such unbalancing can be mitigated by using a multiple-turn structure at lower frequencies. However, due to the self-resonance-frequency (SRF) constraint, most of the transformers can only be implemented in a one-turn fashion at the mm-wave frequency.

To improve the signal balance in our design, the primary and secondary coils are offset to mitigate the capacitive coupling between the primary and secondary coils [128]. The primary coil is also rotated by 45° to further improve balance and more importantly

facilitates the inter-stage routing. Figure 5.16(a) shows the simulated amplitude and phase mismatches versus different offset values at different transformer radiuses. It can be seen that there are multiple solutions which achieve good amplitude and phase balancing simultaneously. The final design parameters should be chosen together with the required coupling coefficient (k) and the primary self-inductance (L) which are plotted in Figure 5.16(b). In this design, an offset distance of 8.5μm and a radius of 32μm are chosen (Figure 5.15). At 84GHz, this offset balun structure achieves an amplitude mismatch of only 0.3dB and a phase mismatch of 2.9° with an SRF of 140GHz.

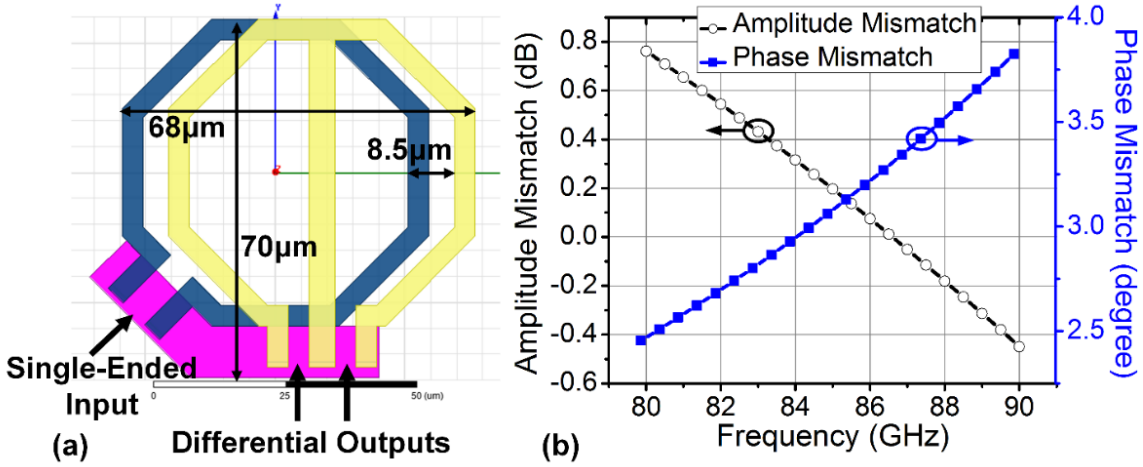

Figure 5.15 – (a) The EM model of the proposed offset transformer-based balun. (b) Simulated amplitude mismatch and phase mismatch of the balun.

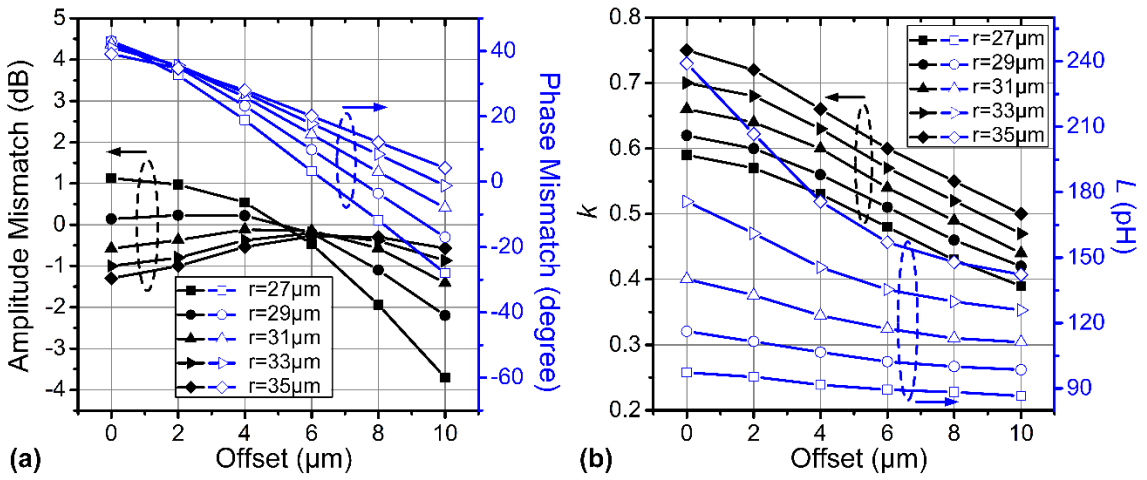

Figure 5.16 – (a) Simulated amplitude mismatch and phase mismatch versus different offset values at different transformer radiuses. (b) Simulated coupling coefficient (*k*) and primary inductance value (*L*) versus different offset values at different transformer radiuses.

The single-ended input of the balun is used as part of the resonance tank in the middle ring oscillator, and the parallel inductance value should be around 140pH to achieve a free-running frequency of 84GHz. If the two differential outputs are well-balanced, the on-chip balun can be modeled using the simplified transformer model [129] shown in Figure 5.17. The desired single-ended input impedance can be obtained by

$$Z_{\text{single}} = j\omega(1-k^2)L + r_{\text{p}} + \frac{k^2}{n^2}(r_{\text{s}} + Z_{\text{diff}})//j\omega k^2 L\,, \tag{5.19}$$

where k is the coupling coefficient, n is the turn ratio, L is the primary self-inductance, r_{p} and r_{s} are the loss resistances in the primary and secondary windings. The differential input impedance of the next stage frequency doubler is (32-j30) Ω, as an equivalent impedance based on a 60Ω resistor parallel with a 30fF capacitor at 84GHz. Figure 18a shows the EM-simulated Z_{single} and the modeled Z_{single} based on (5.19), demonstrating well-matched results. In addition, the EM-simulated and modeled passive losses of the balun are plotted

in Figure 5.18(b). When the balun is loaded by the next-stage doubler, its passive loss is 0.88dB at 84GHz.

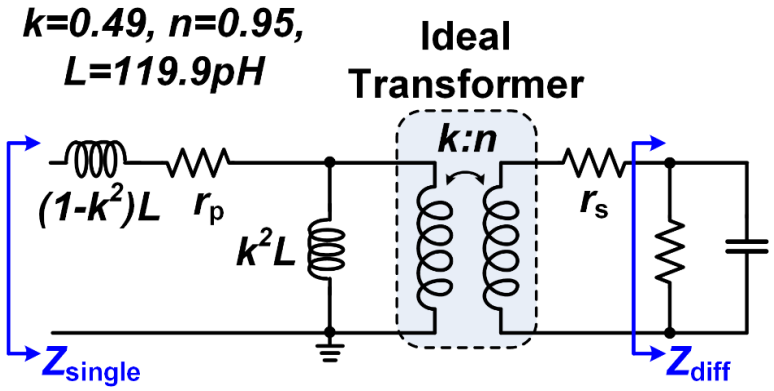

Figure 5.17 – Simplified on-chip balun model.

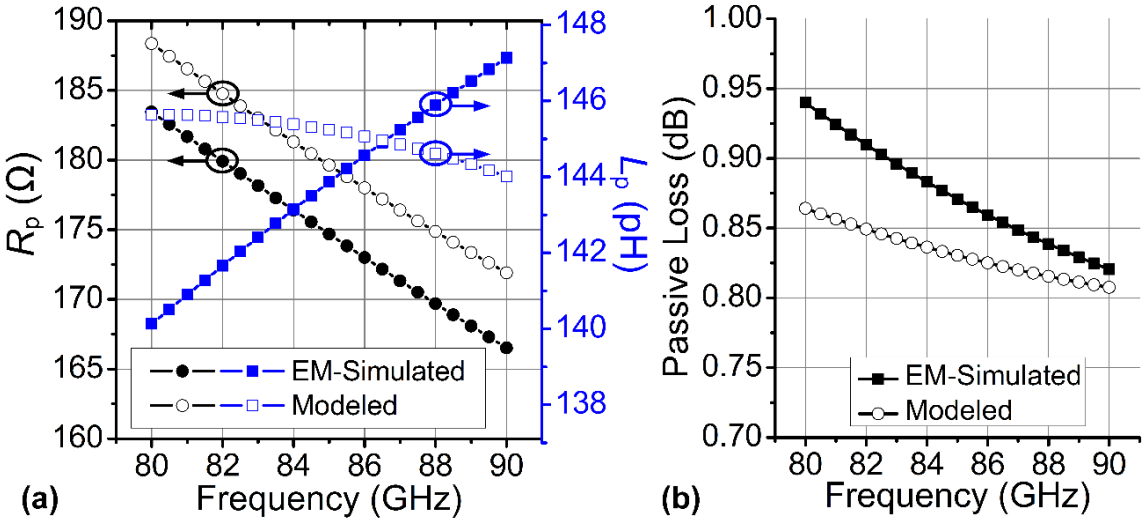

Figure 5.18 – (a) EM-simulated and modeled parallel resistance (R_p) and inductance (L_p) of Z_{single}. (b) EM-simulated and modeled passive loss of the proposed offset balun.

5.3.5 The 3-Phase 42GHz Oscillator (Outermost Ring VCO)

The input stage of the system (the outermost ring), is a 3-phase 42GHz differential ring VCO (120°-mode) designed using the MOSFETs (Figure 5.19). Due to the long T-line routing (660μm), series capacitors are used to reduce the total capacitive loading at the

drain nodes. The differential signals at each stage from the outermost ring are buffered and fed into the 1st stage frequency doubler (Figure 5.9). The doubler is also designed using MOSFETs and biased for optimum 2nd harmonic current generation with Vb_4 of 500mV.

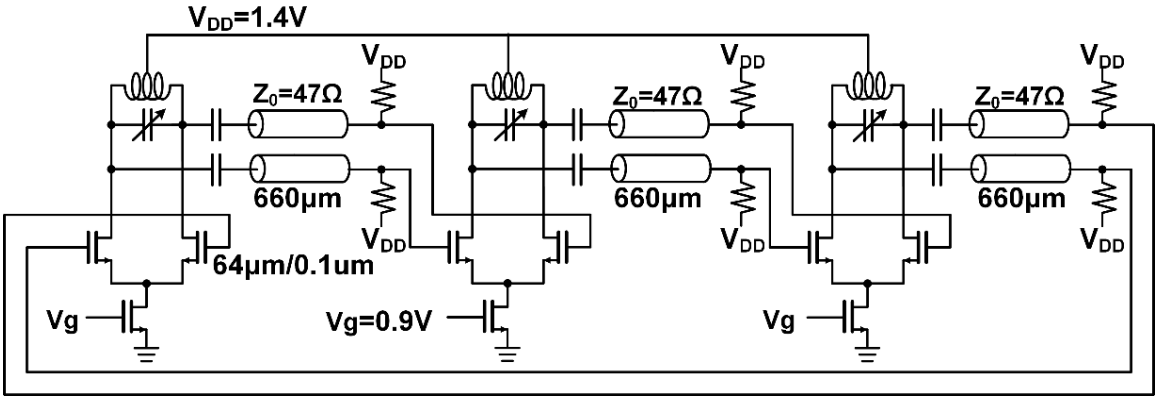

Figure 5.19 – The schematic of the 3-phase 42GHz ring oscillator (outermost ring VCO).

At each stage of the 42GHz ring VCO, the tuning capacitor bank consists of 5-bit binary weighted digital controls (C_0 – C_4) for discrete tuning and 1 varactor for continuous tuning. The simulated tuning range of the VCO is plotted versus the bias voltage of the varactor (VCTRL) under different digital control settings in Figure 5.20(a). A total frequency tuning range from 38.8GHz to 42.5GHz (9.1%) is achieved. The phase noise of the VCO is within -105dBc/Hz to -107dBc/Hz across the tuning range. Figure 20b shows a simulated phase noise plot for all the ILO stages when the system is locked to the outermost ring VCO. Since the frequency multiplication factor is 2 from the outermost ring to the middle ring and also 2 from the middle ring to the innermost ring, the phase noise is thus 6dB higher for the middle ring, and 12dB higher for the innermost ring compared with the outermost ring. The final THz output is the 3rd harmonic output of the innermost ring, which thus has 21.5dB (20×log12) phase noise degradation compared with the outermost ring VCO. At 1MHz frequency offset, the final output has a simulated phase noise of -

85.1dBc/Hz, showing the expected phase noise degradation due to the cascaded frequency multiplication.

5.4 Measurement Results

The chip microphotograph and a photo of the measurement setup are shown in Figure 5.21. The DC pads and digital controls are directly wire-bonded to an open-top chip carrier mounted on an FR4 PCB. The core area of the chip is 720µm by 700µm. The 3-stage "active frequency multiplier" chain multiplies a 42GHz signal to generate the 504GHz output. The outermost ring VCO draws 122mA from 1.4V. The middle ring ILO draws 113-129mA from 1.6V, and the innermost ring ILO draws 24-32mA from 1.5V within the system frequency tuning range.

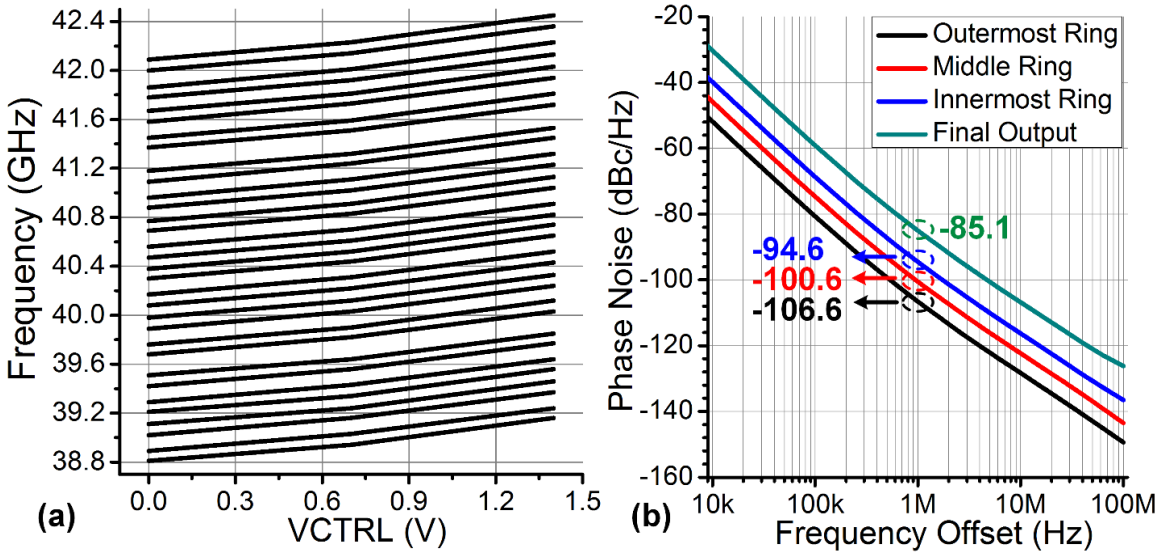

Figure 5.20 – (a) The frequency tuning range of the outermost ring VCO. (b) Simulated phase noise of each ring oscillator and the final THz output when the system is locked to the outermost 42GHz ring VCO.

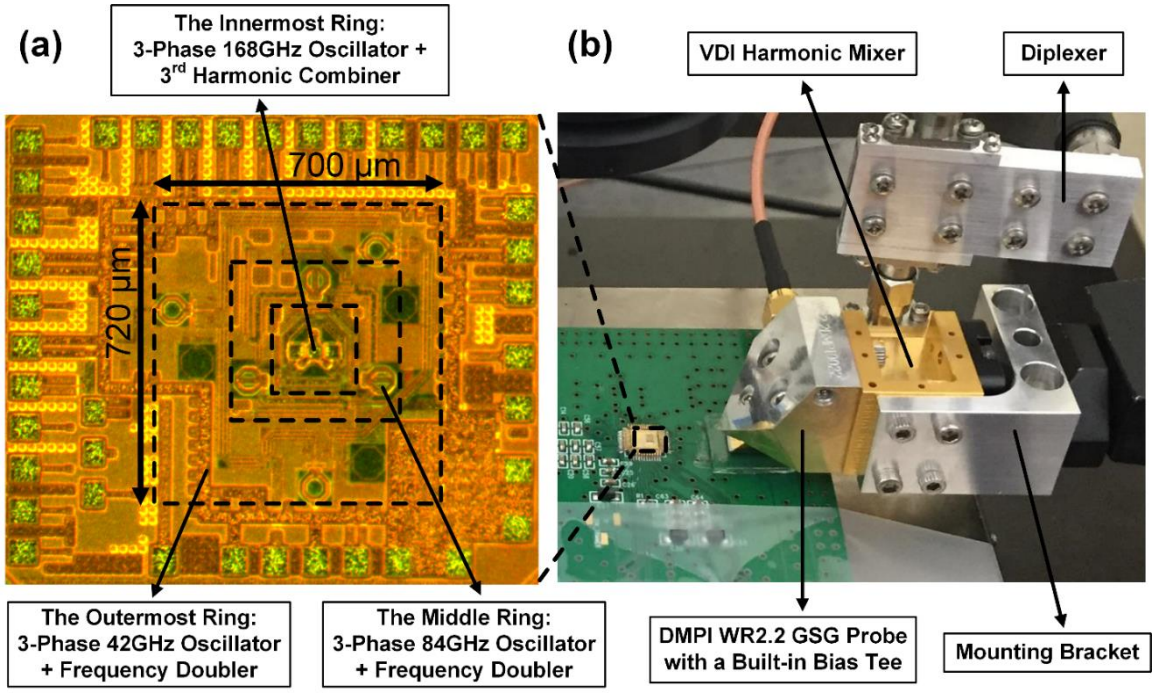

Figure 5.21 – (a) Chip microphotograph. (b) Photograph of the spectrum measurement setup including the probe and the down-conversion harmonic mixer.

Since the output GSG pads are in the middle of the chip, the prototype is directly measured through wafer probing. In a practical application, the chip can be flip-chip packaged to connect to the antenna in package (AiP) [130], so that the signal can be radiated out. Alternatively, silicon-based micromachined waveguides [131], [132] can be used to guide the THz signal from the chip. Figure 5.22 shows the simplified setups for the spectrum and the power measurements. The output 500GHz signal is probed by a DMPI WR2.2 GSG probe with a built-in bias tee [133]. First, the frequency measurement is performed by down-converting the 500GHz tone with a VDI WR2.2 EHM harmonic mixer. The harmonic mixer uses the 16th harmonic of the LO signal which is provided from a Keysight signal generator. After the frequency down-conversion, the IF signal is amplified by an IF amplifier and captured with a spectrum analyzer. A typical IF spectrum is shown in Figure 5.23(a) with a clean spectrum when all the three oscillators are locked.

The 500GHz signal tone is identified by sweeping the LO frequency and observing the corresponding change in the IF frequency. However, at the edge of the frequency locking range, 2 tones will arise at the output IF spectrum shown in Figure 5.23(b), indicating an undesired quasi-locking behavior. To demonstrate the total frequency tuning range, the measured output frequency is plotted in Figure 5.24 with the corresponding capacitor bank settings of the outermost ring VCO together with Vb_1 and Vb_2 (Figure 5.9). A frequency tuning from 485.1 to 510.7GHz is achieved (with a total 5.1% tuning range). This is the largest frequency tuning range among all the reported Si-based THz oscillator sources in the 500GHz band.

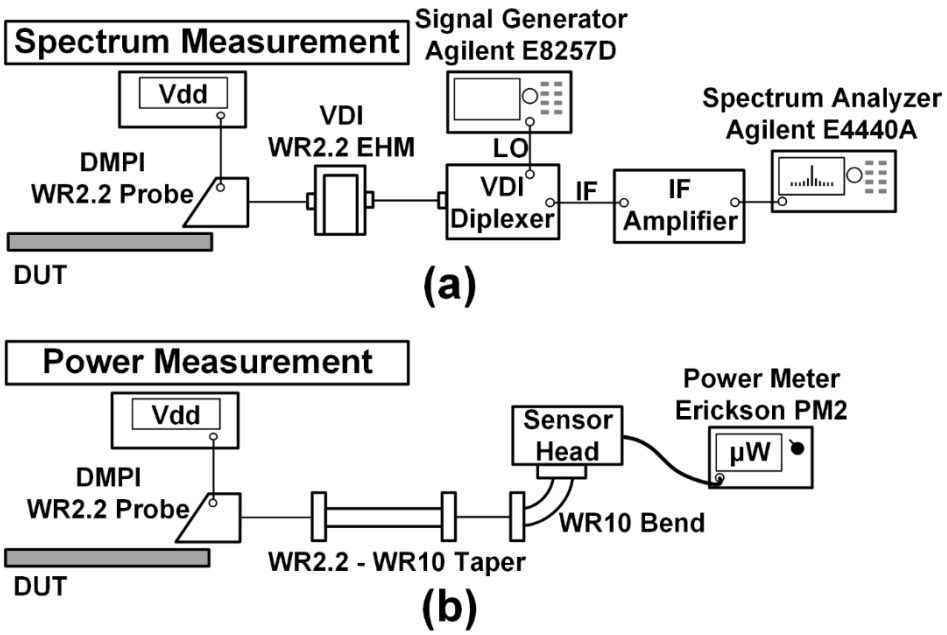

Figure 5.22 – (a) Spectrum measurement setup. (b) Power measurement setup.

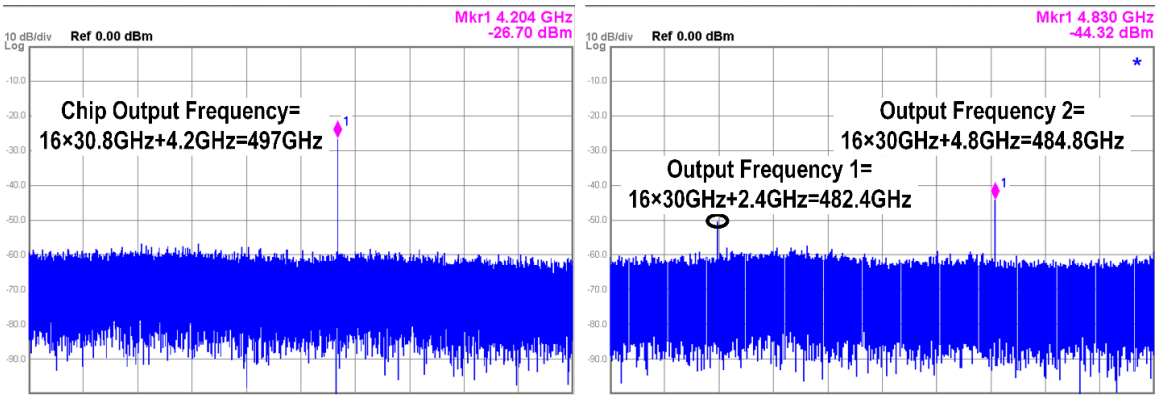

Figure 5.23 – (a) A typical measured output spectrum (with IF amplifier) after down-conversion by the 16th harmonic of the LO (LO=30.8 GHz). (b) At the edge of locking range (LO=30GHz), it shows 2 tones on the spectrum analyzer, demonstrating an undesired quasi-locking behavior.

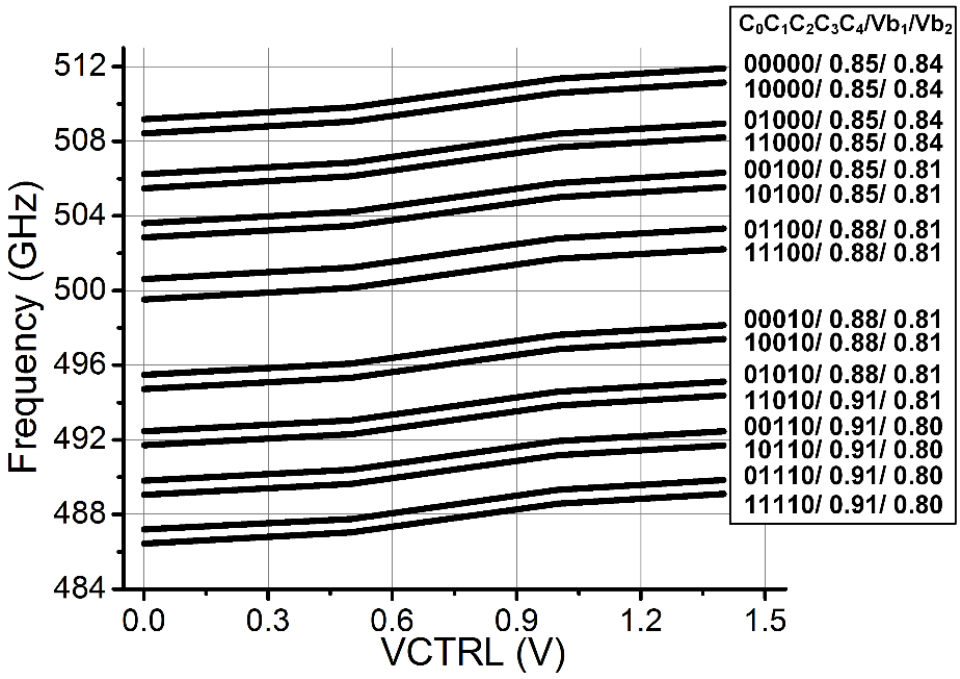

Figure 5.24 – Measured output frequencies versus varactor's tuning voltage (VCTRL) under different digital control settings (C_0 – C_4) together with Vb_1, Vb_2 settings.

As mentioned previously, the frequency ranges of the three oscillators are designed to ensure their mutual locking. To verify the mutual locking of the three oscillators in the measurements, the following checking has been performed. First, from the output

frequency perspective, the digital setting and the varactor's tuning voltage (VCTRL) of the outermost ring VCO are changed, and the corresponding frequency change of the final output is observed. However, if we only change the biasing voltages of the inner two ring ILOs (Vb_1 and Vb_2), the output frequency remains the same. This directly verifies that the 3 ring oscillators are locked together, and the final output frequency is determined only by the outermost ring VCO. Secondly, from the phase noise perspective, the phase noise of the final output is -87dBc/Hz at 1MHz offset at the output frequency of 501GHz [Figure 5.25(a)] when the 3 ring oscillators are mutually locked. The outermost ring VCO is then turned off and the phase noise is measured again. The output frequency shifts from 501GHz to 497.8GHz and the phase noise degrades to -75.6dBc/Hz at 1MHz offset [Figure 5.25(b)], which is now limited by the innermost ring oscillator. Thirdly, the output phase noise is also measured and compared with the simulated phase noise of the outermost ring VCO (Figure 5.26) across the frequency tuning bandwidth. Theoretically, phase noise of the 504GHz tone should have a 21.5dB (20×log12) degradation compared with the 42GHz tone. The measured phase noise difference matches well with this theoretical prediction within a 5.1% locking range, indicating the proper injection locking of the 3-stage oscillators. Note that this 5.1% locking range is used to determine the system frequency turning range. On the other hand, the output phase noise degrades substantially when the oscillators are not locked, i.e., beyond the locking range.

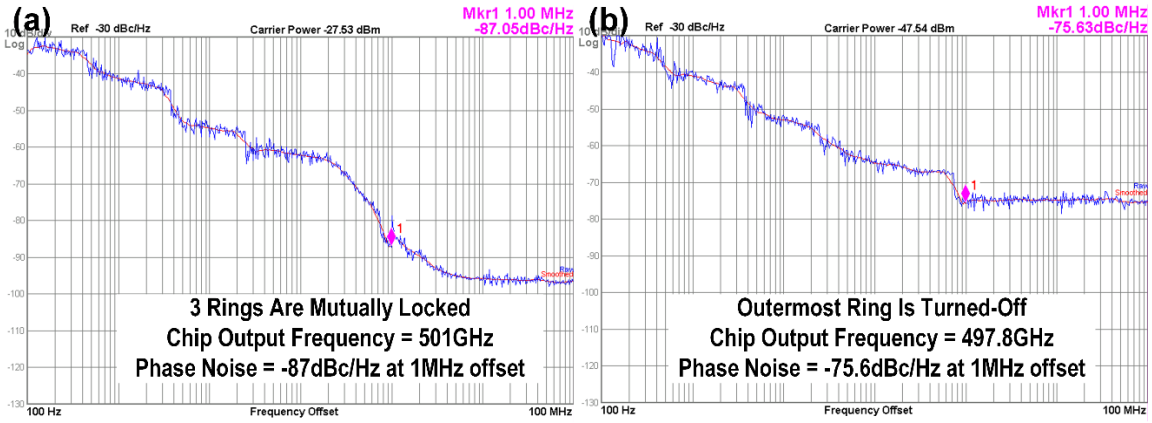

Figure 5.25 – (a) Measured phase noise at chip output frequency of 501GHz when 3 rings are mutually locked. (b) Measured phase noise when the outermost ring is turned off. The final output frequency shifts from 501GHz to 497.8GHz, and its phase noise degrades to -75.6dBc/Hz at 1MHz offset.

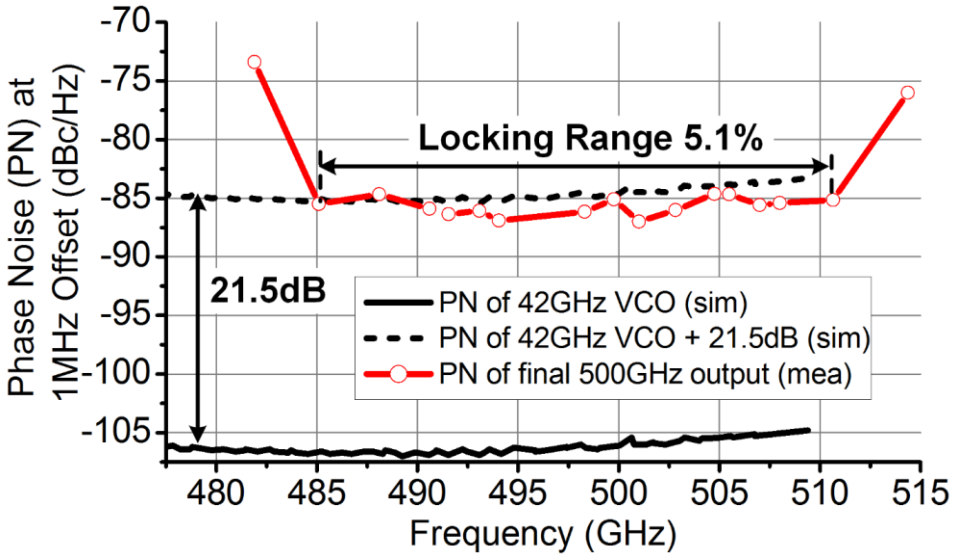

Figure 5.26 – Simulated phase noise of the outermost ring (42GHz VCO), and measured phase noise of the final 500GHz output at 1MHz offset.

In the power measurement, the probed output signal is first filtered by a WR-2.2 waveguide. This suppresses any signal outside of 325-500GHz, e.g., the fundamental tone of the 168GHz oscillator. The signal is then detected by an Erickson PM2 power meter. The loss of the WR2.2 probe is 5dB at 500GHz [133], the loss of the taper is 0.6dB, and the loss of the waveguide bend is 0.4dB according to VDI application note [134]. The

measured output power versus frequency is shown in Figure 27, verifying the broadband performance at 500GHz. The peak output power drops 3.3dB compared with the simulation. The difference between the simulation and measurement may be due to the inaccuracy of transistor model at this frequency.

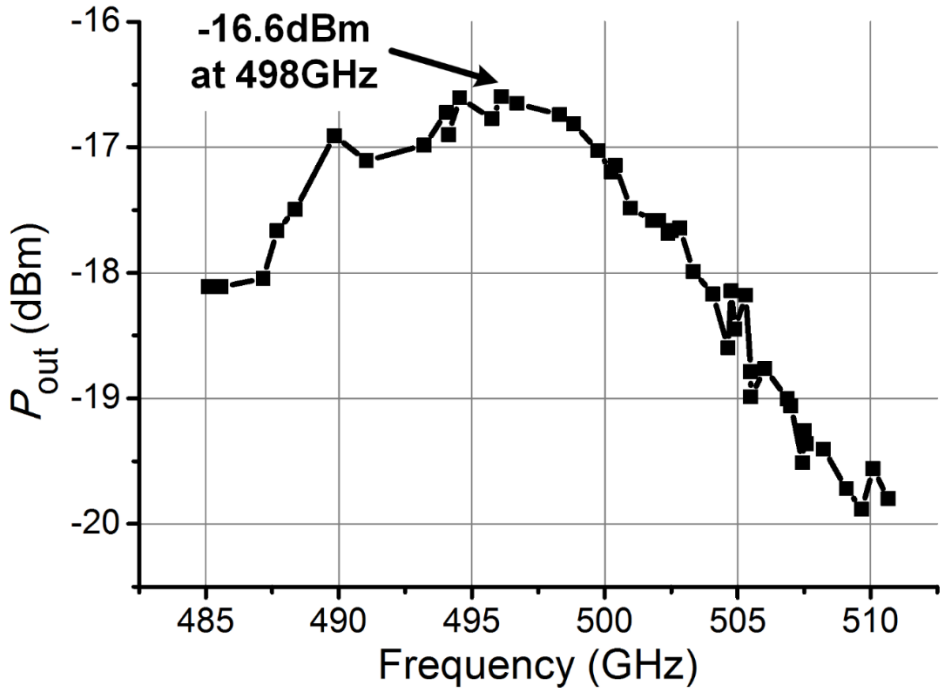

Figure 5.27 – Measured output power versus frequency.

5.5 Chapter Summary

This chapter presents a multi-phase injection locking (IL) technique and its application in the locking range extension in multi-phase ILOs for THz signal generation. Based on the multi-phsae IL technique and sub-harmonic ILOs, an "active frequency multiplier chain" architecture is proposed to achieve scalable THz signal generation. A cascaded 3-stage 3-phase 2nd-order sub-harmonic ILO chain is implemented in the IBM 9HP SiGe BiCMOS process to generate THz signals in the 500GHz band. A frequency tuning range of 5.1% and a phase noise of -87dBc/Hz at 1MHz offset are achieved, which

are the largest frequency tuning range and the best phase noise among the reported silicon-based THz oscillator sources at 0.5THz. In addition, this design generates a maximum output power of -16.6dBm at 498GHz, and it achieves more than -20dBm across the entire system frequency tuning range. A performance comparison of silicon-based THz oscillator sources is summarized in Table 5.1.

Table 5.1 – Comparison with state-of-the-art silicon-based THz oscillator sources.

Reference	Center Frequency (GHz)	CW Tuning Range	P_{out} (dBm)	Phase Noise at 1MHz (dBc/Hz)	Technology
This work	**498**	**5.1%**	**-16.6**	**-87**	**90nm BiCMOS**
JSSC 11	482	N/A	-7.9	-76	65nm CMOS
ISSCC 14	528	3.2%	-11.3†/0†,*	N/A	130nm BiCMOS
JSSC 14	540	4.0%	-31/-33.1†	N/A	40nm CMOS
VLSI 11	553	N/A	-36.5†	N/A	45nm CMOS
ISSCC 14	256	6.5%	4.1	-94	65nm CMOS
JSSC 13	260	1.4%	0.5†	-78.3	65nm CMOS
JSSC 12	280	3.2%	-7.2†,*	N/A	45nm SOI
JSSC 13	288	1.4%	-1.5/-4.1†	-87	65nm CMOS
JSSC 12	290	4.5%	-1.2	-78	65nm CMOS
ISSCC 14	290	7.9%	-14	-82.5	90nm BiCMOS
JSSC 13	316	1.9%	-21	N/A	45nm SOI
JSSC 13	317	5%	-13.3	-78	120nm BiCMOS
JSSC 12	320	2.6%	-3.3	-77	65nm CMOS
ISSCC 14	338	2.1%	-0.9†	-93	65nm CMOS

† Radiated power from on-chip antennas. * P_{out} generated by 16-element array.

CHAPTER 6. A PACKAGED TRANSCEIVER CHIPSET IN CMOS FOR FULL-BAND CONTINUOUS-WAVE MILLIMETER-WAVE AND TERAHERTZ HYPERSPECTRAL IMAGING

6.1 Introduction

Mm-wave/THz hyperspectral imaging has numerous applications in security, non-destructive evaluation, material characterization, and medical diagnostics [135]. Unlike single-frequency imaging, hyperspectral imaging operates over a wide frequency range and offers spectroscopic information on each imaging pixel. This combines mm-wave/THz high-resolution imaging with spectroscopy and improves detection sensitivity and specificity. In practice, pulse-based imaging supports fast data acquisition but requires receiver (RX) with real-time wideband sampling (>50GHz). Such instantaneous broadband imaging modality inevitably exhibits severely degraded sensitivity (due to integrated noise) and requires high-end signal sampling, both of which make it very challenging to achieve a low-cost SoC solution. On the other hand, continuous-wave (CW) imaging supports better sensitivity, especially using coherent detection method with a low IF bandwidth [137]–[140]. Its operation allows for the use of simplified heterodyne receiver, enabling silicon-based implementation of the entire imaging system. However, there are limited mm-wave/THz integrated electronics available that support CW hyperspectral imaging with large bandwidth (BW), sufficient output power (P_{out}), and high sensitivity. Some existing CW transmitters (TX) use the harmonics for wideband coverage, which cannot support full-band scanning at any frequency in the band [137]. In this chapter, a full-band CW TX/RX chipset is proposed to realize a generic hyperspectral imaging system without

knowing the particular band of interest, we therefore optimize its performance to achieve flat TX P_{out} and RX conversion gain (CG) over a broad BW. Our mm-wave/THz hyperspectral imaging system comprises a 90-300GHz TX with a ±2dB P_{out} variation using a distributed quadrupler architecture and a 115-325GHz 4th sub-harmonic coherent RX with -115dBm sensitivity (1kHz RBW) using high-order filter-based matching networks (MNs). The TX and RX chips are flip-chip integrated with wideband vivaldi antennas on low-cost organic LCP substrates. This packaged wideband system offers a promising solution for low-cost field-deployable hyperspectral imaging.

6.2 Ultra-Broadband TRX Implementation

To achieve wideband THz signal generation, a distributed quadrupler (DQ) scheme is proposed as the imaging TX (Figure 6.1). Distributed topologies can absorb the device parasitic capacitors into the input/output synthetic T-lines and allow for broadband power combining from each stage [141]. Each DQ stage comprises 4 transistors driven by differential quadrature signals (±I and ±Q) at the fundamental frequency f_0. The input differential I/Q signals propagate through matched gate T-lines, drive the DQ stages, and generate even-order harmonics. The drain T-line achieves broadband matching (>400GHz), and the simulated 3dB insertion loss BW of the loaded 10-stage drain T-line is 327GHz (Figure 6.1). Moreover, to ensure constructive combining of the forward $4f_0$ signals among the DQ stages, the group delay of the $4f_0$ signal between the adjacent DQ stages on the drain T-line is designed to be equal to that of the f_0 signal on the gate T-line over the TX BW. Two 10-stage DQs driven by differential I or Q signals are in-phase combined at the antenna input port to boost the $4f_0$ output signal and cancel the $2f_0$ harmonic.

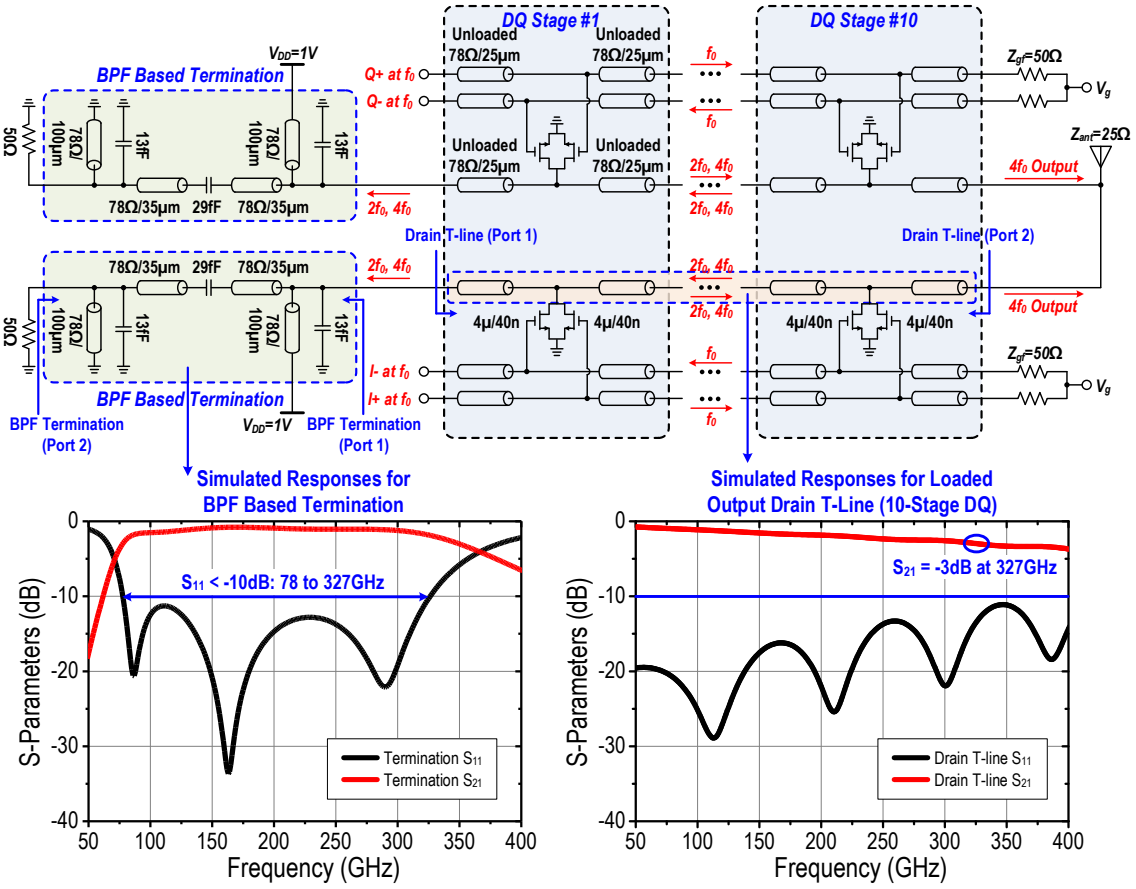

Figure 6.1 – Circuit schematic of the 10-stage distributed quadrupler (DQ) as the 90-300GHz TX, and the simulated return loss (S_{11}) and insertion loss (S_{21}) for the BPF based termination and the loaded output drain T-line. The gate/drain T-line characteristic impedance is 78Ω without DQ loading and 50Ω with DQ loading.

In conventional DAs, the DC supply feed is through on-chip chokes or an off-chip bias-tee via the output pad. However, for this 90-300GHz DQ TX, it is difficult to realize any on-chip choke, while off-chip bias-tees will complicate the TX-antenna packaging. Thus, an on-chip 0.5dB ripple 3rd-order Chebyshev bandpass filter (BPF) is inserted between the on-chip termination resistor and the drain output of the 1st stage DQ. This BPF provides a broadband termination of the backward waves and a DC supply feed point through its shunt T-line (Figure 6.1). The broadband differential I/Q inputs for the DQ are generated by an on-chip Marchand balun and a transformer-based quadrature generation

network (Figure 6.2). At f_0=60GHz, the EM-simulated total average passive loss of the input network is 2.5dB with a 6dB inherent loss due to 1:4 power dividing. The ±1dB amplitude mismatch BW is from 38-84GHz (1:2.2), and the 5° phase mismatch BW is from 35-82GHz (1:2.3), achieving matched and broadband I/Q driving signals.

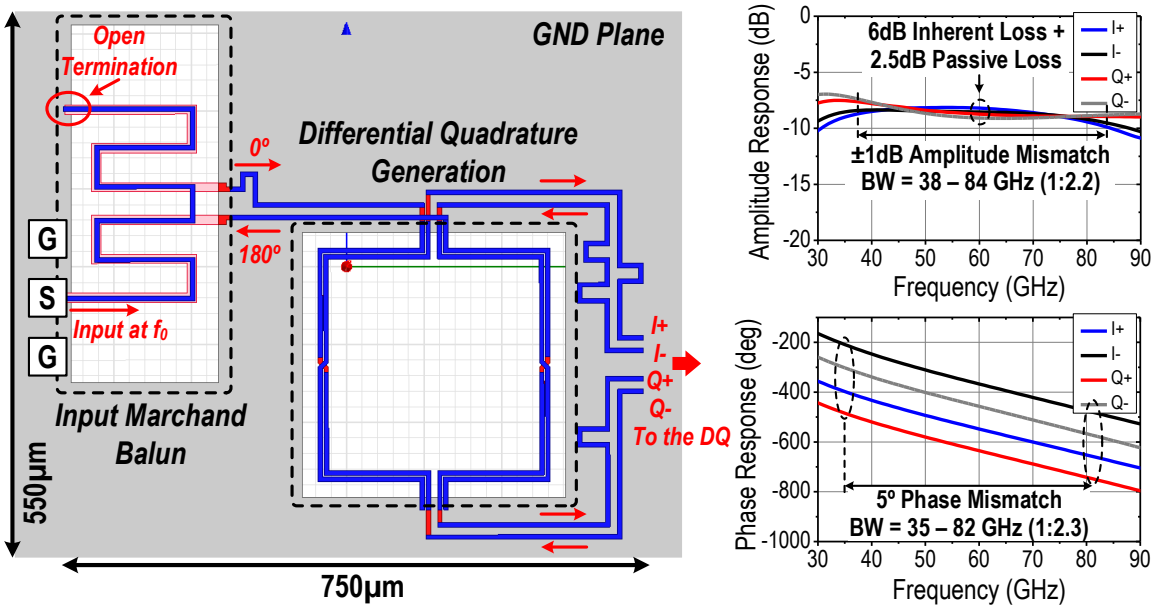

Figure 6.2 – The 3D EM model of the input Machand balun and the differential I/Q generation network, and the EM-simulated amplitude/phase responses of the four quadrature outputs at f_0.

The wideband RX employs a 4th sub-harmonic mixing (SHM) topology using an anti-parallel diode pair (APDP) [140]. Compared with power detectors, this coherent heterodyne detection achieves a much higher sensitivity and SNR using low-IF operation, obviating the need of high-power illumination sources in imaging. In this 4th SHM RX, the received signal is mixed with the 4th LO harmonic, which reduces the required LO power and frequency to be 7dBm and <82GHz. By absorbing the APDP parasitic capacitors into two 4th-order Chebyshev BPF MNs in the LO and RF paths, a large RX BW, low conversion loss, and high out-of-band rejection are achieved (Figure 6.3). The BW of the

4th-order Chebyshev BPF is proportional to g_5/Q, where Q is the APDP loaded quality factor, and g_5 is the load coefficient in the normalized filter prototype. A larger g_5 provides a larger BW but introduces in-band ripple. In this RX, a 0.5dB ripple is chosen with g_5=1.98 to ensure RX CG flatness. This also inherently applies a 1:2 impedance transformation to match the RX 50Ω input with the APDP parallel resistance. The IF output is amplified by an on-chip LNA and an open-drain buffer.

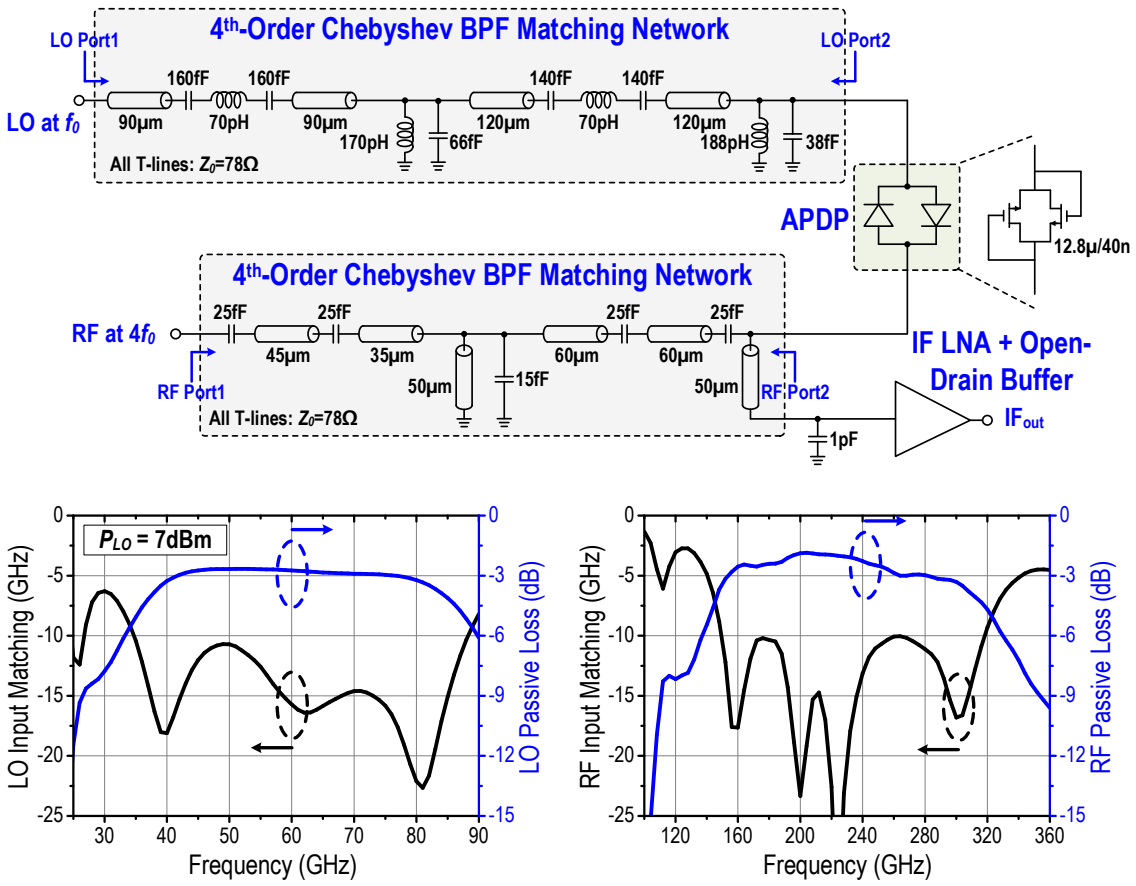

Figure 6.3 – Circuit schematic of the 4th sub-harmonic mixing (SHM) as the 115-325GHz RX, and the simulated responses for the LO path and RF path 4th-order Chebyshev BPF matching networks (MNs).

6.3 Measurement Results

A proof-of-concept 10-stage DQ TX and a 4th SHM RX are implemented in a 45nm CMOS SOI process (Figure 6.4). For RX characterization, the IF frequency is set as 250MHz with 1kHz RBW (corresponding to 1ms time constant) on the spectrum analyzer. The measured RX CG is between -3dB and 1dB in 115-325GHz with an LO power of 7dBm±1dB (Figure 6.5). The RX CG can be further boosted by integrating an extra high-gain IF amplifier on-chip. The single sideband (SSB) noise figure (NF) is calculated from the measured noise floor at the IF output and the CG [140]. The measured SSB NF is 29-37dB across the RX band. The sensitivity at the RF input is defined as K_B•T•BW•NF with BW=1kHz. A sensitivity of -107 to -115dBm is achieved in 115-325GHz, demonstrating the broadband high-sensitivity of the coherent RX. For the TX characterization, Figure 6.5 shows the simulated and measured TX P_{out}. At center frequency 200GHz, TX P_{out} is -11dBm with 18dBm P_{in} at 50GHz. TX P_{out} flatness is within ±2dB for 90-300GHz, out-performing any reported mm-wave/THz TX in silicon. The 300GHz high-end frequency is limited by the drain T-line loss, while the 90GHz low-end frequency is due to the imbalance of the I/Q driving signals. An on-chip 22.5-75GHz DA (with 18dBm P_{out}) can be integrated as the TX source for full system integration [141]. The measured TX P_{out} vs. P_{in} is shown in Figure 6.5 with the maximum TX P_{out} of -6dBm at 20dBm P_{in}.

The wideband TX and RX are flip-chip packaged to a 2-mil LCP substrate with on-package 100-280GHz vivaldi antennas (Figure 6.4). Transmission mode hyperspectral imaging is performed with the measurement setup shown in Figure 6.6. The object is moved by a step-motor-controlled 2D linear translation stage. PTFE lens are used to focus the beam. Hyperspectral images of a cookie and a screw inside a translucent package at

multiple frequencies are shown in Figure 6.7. The mm-wave/THz images clearly delineate the cookie and the screw inside the package, which is useful in nondestructive and non-contact food safety screening. Hyperspectral images of a dry leaf and a fresh leaf at multiple frequencies are presented in Figure 6.8, showing water content difference in dry and fresh leaves.

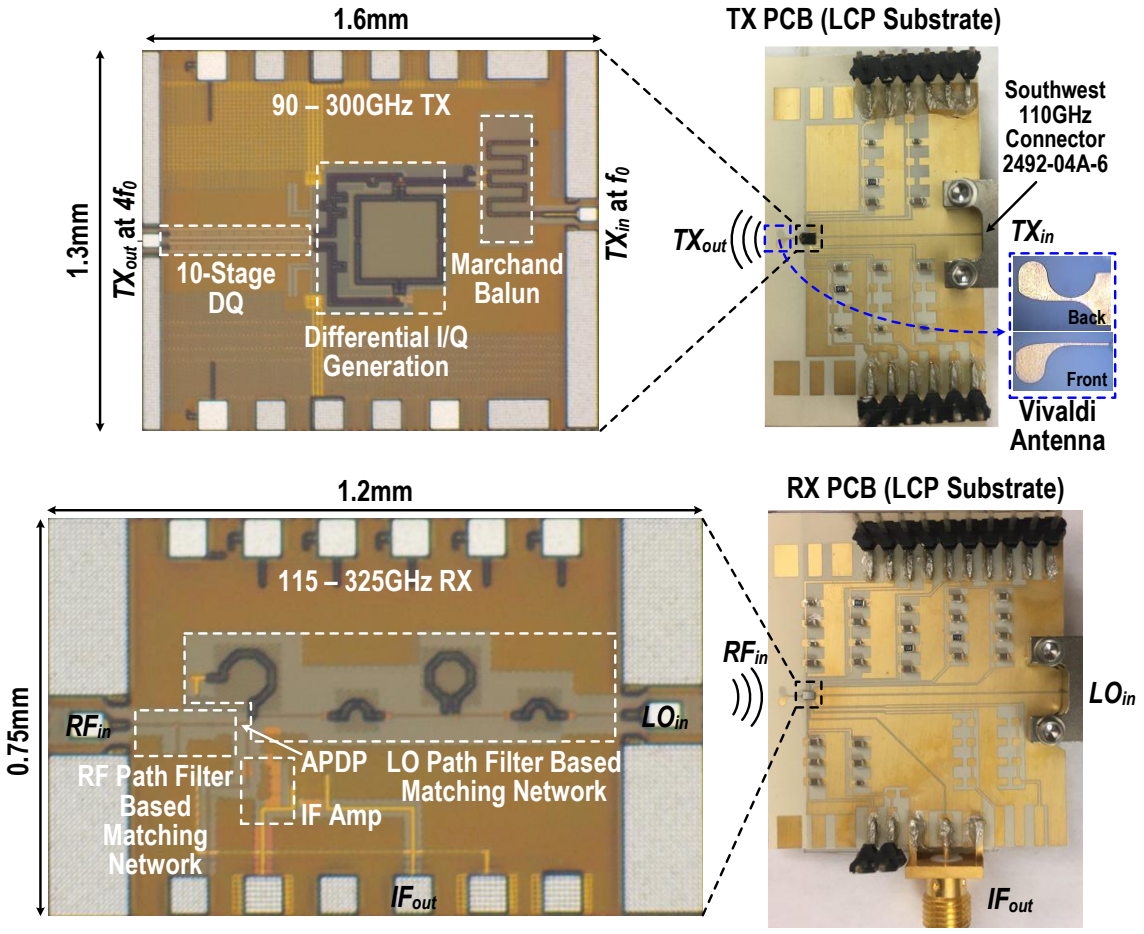

Figure 6.4 – Chip microphotographs and pictures of the packaged TX/RX chips and modules.

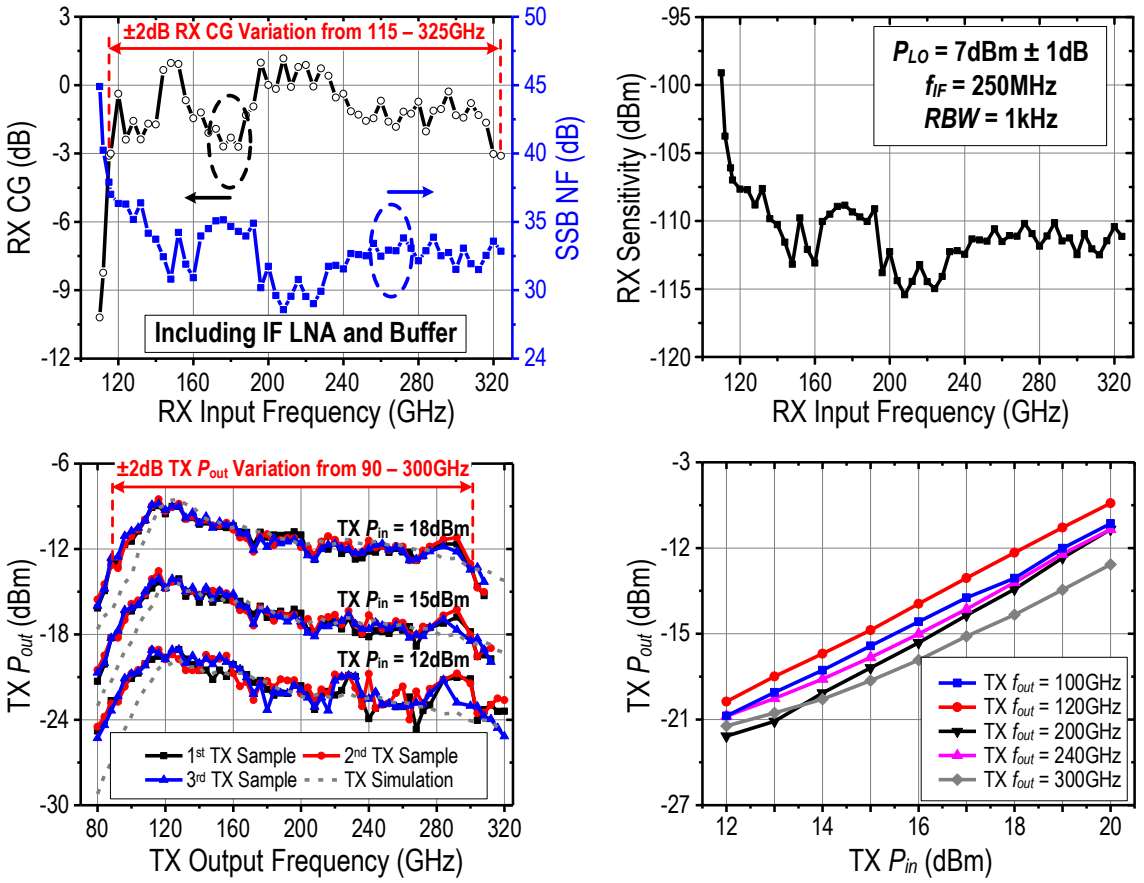

Figure 6.5 – Measured RX CG, SSB NF, and sensitivity versus frequency including on-chip IF LNA and buffer. Measured TX P_{out} versus frequency for 3 independent samples at P_{in} = 12, 15, and 18dBm, and measured TX P_{out} versus P_{in} at different TX output frequencies.

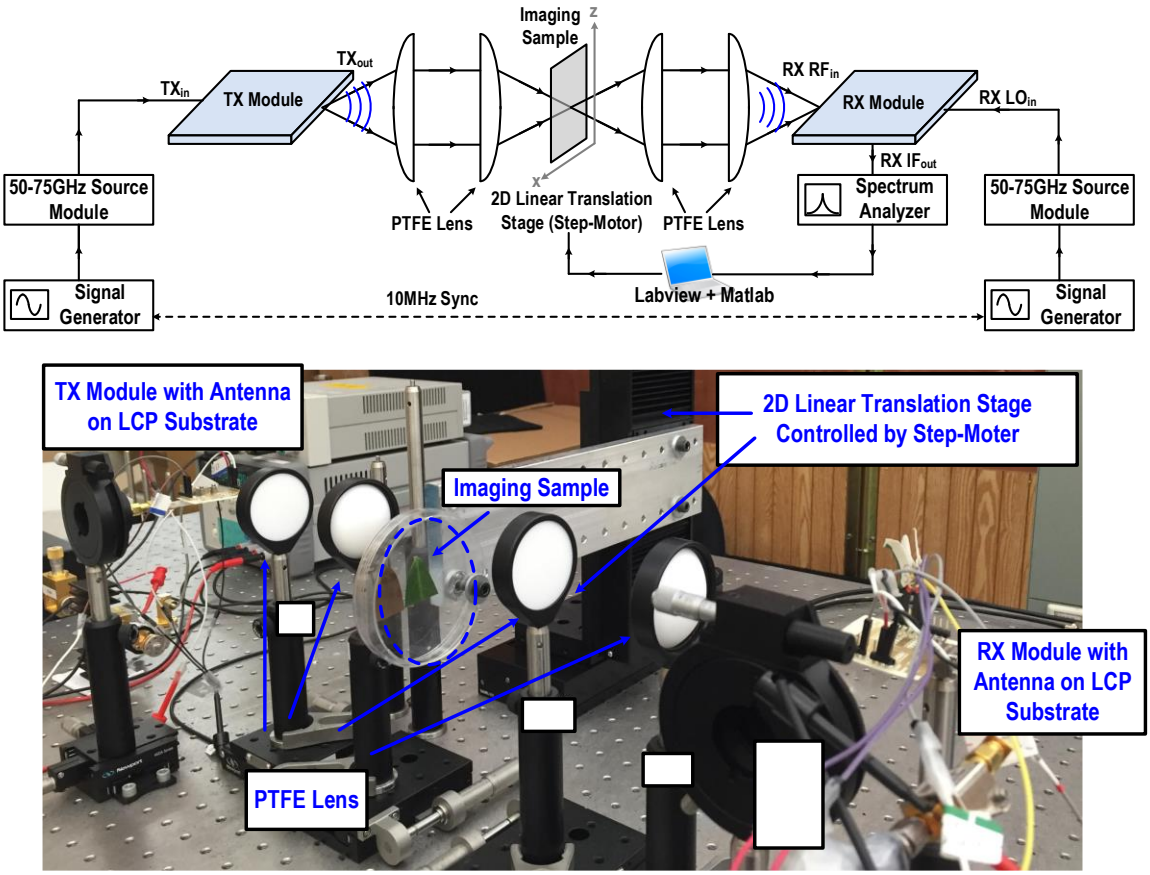

Figure 6.6 – Measurement setup for transmission mode hyperspectral imaging. The object is moved by a step-motor-controlled 2D linear translation stage. Additional absorbers are used in the measurements but are not shown in this picture for clarity.

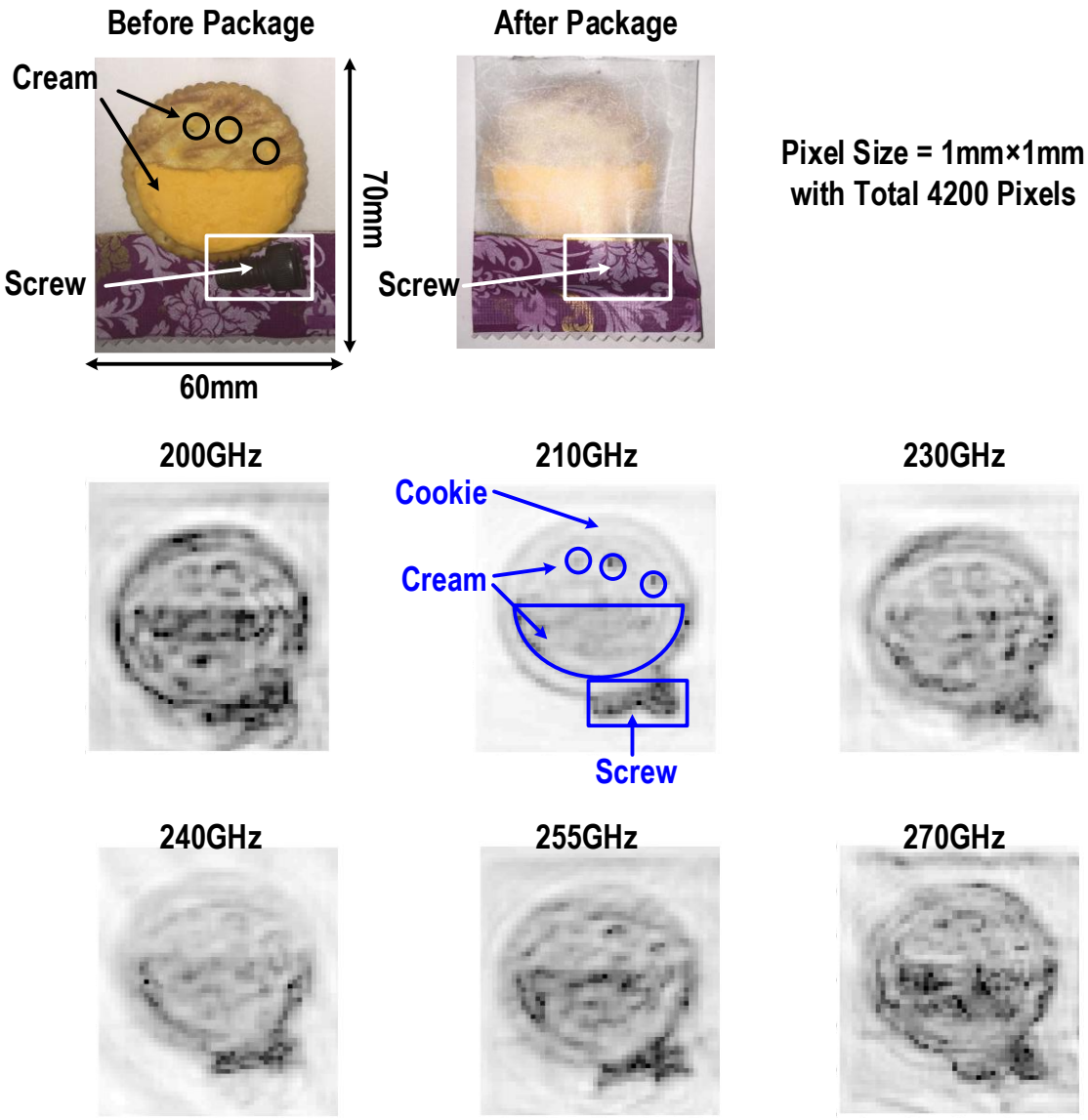

Figure 6.7 – Full-band hyperspectral images of a cookie and a screw inside a translucent package for food safety screening at 200, 210, 230, 240, 255, and 270GHz.

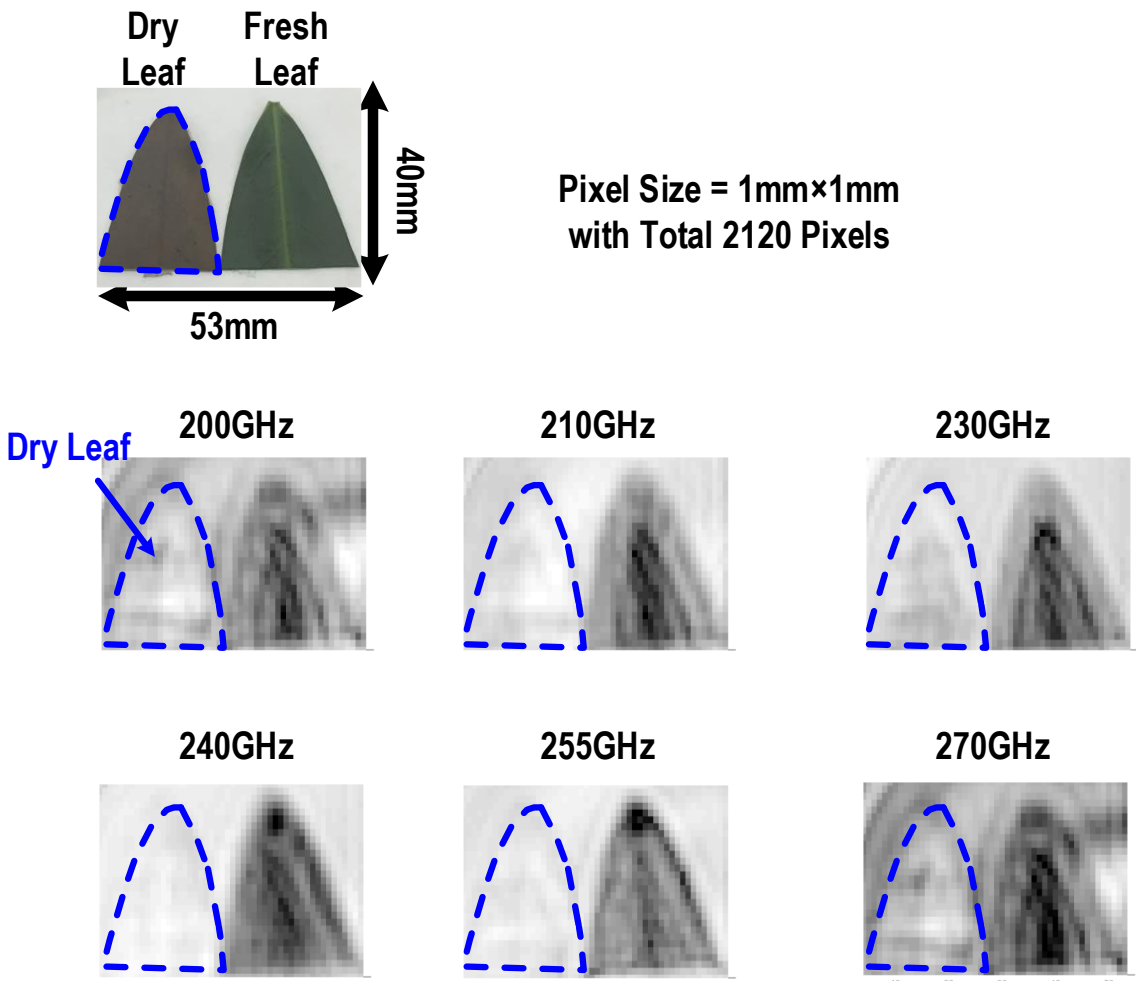

Figure 6.8 – Hyperspectral images of a dry leaf and a fresh leaf at 200, 210, 230, 240, 255, and 270GHz, showing water content difference in dry and fresh leaves.

CHAPTER 7. CONCLUSION

In this dissertation, we discussed our approaches towards the development of fully integrated signal generation and detection systems for various emerging applications at mm-wave and THz, such as high-speed wireless communication, Internet-of-Things (IoT), "invisible" field-deployable sensor networks, radar, spectroscopy, and hyperspectral imaging. Signal generation and detection in silicon is challenging due to the limited supply voltage, lower cut-off frequency compared with compound III-V processes, and lossy on-chip passive components. We have presented several new system architectures and circuit techniques to overcome these limitations and demonstrated the state-of-the-art system performance.

First, we propose a multi-feed antenna structure that synthesizes the desired far-field radiation characteristics with high-efficiency direct on-antenna power combining. The multiple antenna feeds are driven simultaneously, and the driving signals are scaled with proper amplitudes/phases which together actively synthesize the desired on-antenna RF current/voltage distribution, achieving the resulting desired far-field radiation pattern. Compared to power combining using on-chip/on-package passive networks, the on-antenna power combining is much more efficient. It also provides the flexibility to optimize the antenna driving impedance based on the locations of the antenna feeds. Compared to spatial power combining using antenna arrays, it is capable of boosting the total radiated power in only one antenna footprint and maintaining the field-of-view as a conventional single-feed antenna. Based on the proposed multi-feed antenna, we implemented a 60GHz on-chip linear radiator, as a 4-feed slot antenna driven by 16 unit PAs, demonstrating the unique advantages of antenna-electronics co-design and highest output power compared

with the reported 60GHz power amplifiers (PAs) in silicon. The on-chip radiator also supports multi-Gb/s complex modulations in dynamic operations.

Secondly, we present a 60GHz full-duplex (FD) transceiver front-end with an on-chip multi-feed self-interference-canceling (SIC) antenna and an all-passive canceler. The multi-feed SIC antenna provides a high TX-RX isolation (>35dB in measurement), an instantaneous broad bandwidth (60-75GHz), and no additional TX/RX-path signal loss, in only one antenna footprint. The all-passive zero-power RF canceler supports large dynamic range and nearly orthogonal amplitude/phase tuning, particularly suitable for mm-wave FD massive MIMOs, where each RX element requires multiple cancelers to suppress its self-/neighbor-interferences. As proof of concept, two FD TRX front-end chips are used to establish a 4Gb/s FD wireless link before using any digital-domain SIC, which is the first mm-wave FD link that supports Gb/s complex modulated signals simultaneously through the TX and RX.

Next, we report an exploratory study on using CMOS low-power THz radios to support high-quality short-range wireless link. A THz pico-radio concept is proposed that achieves extreme radio miniaturization to enable future “invisible” field-deployable sensor network and IoT applications. Compared with the reported silicon-based 300GHz TRXs, this bidirectional THz pico-radio achieves the lowest maximum DC power (49.7mW) and the longest communication distance (50cm) without any silicon lens. Compared with reported low-power radios at MHz, GHz, and mm-wave frequencies, it also achieves the highest radio miniaturization (>7.8× radio size reduction), highest data rate (maximum 16Mb/s 16-ary ASK signals with BER<10^{-5}), best energy/bit FOM, and competitive DC power consumption. This THz pico-radio will enable a wide variety of distributed sensing

applications, such as very-large-scale position/motion tracking, THz-range temperature/humidity monitoring, vibration/deformation sensing, and non-contact THz electromagnetic “tactile sensing”.

In addition, we present a multi-phase sub-harmonic injection locking technique and its application in the locking range extension in multi-phase injection locking oscillators for THz signal generation. Based on this technique, a scalable “active frequency multiplier” chain architecture and a multi-ring system topology are proposed to generate the desired THz signal from a low mm-wave frequency or RF reference source. We demonstrated a cascaded 3-stage 3-phase 2^{nd}-order sub-harmonic injection locking oscillator chain in an advanced 90nm SiGe BiCMOS process, achieving the largest frequency tuning range (5.1%) and the best phase noise (-87dBc/Hz at 1MHz offset) among all the reported silicon-based THz oscillator sources at 0.5THz.

The last part of this dissertation introduces a full-band continuous-wave transceiver chipset for mm-wave/THz hyperspectral imaging. Hyperspectral imaging operates over a wide frequency range and offers spectroscopic information on each imaging pixel, which improves imaging sensitivity and specificity. The imaging system comprises a 90-300GHz TX with a ±2dB output power variation using a distributed quadrupler architecture and a 115-325GHz 4^{th} subharmonic coherent RX with -115dBm sensitivity (1kHz RBW) using high-order filter-based matching networks. Transmission mode hyperspectral images are successfully demonstrated at multiple frequencies in band for non-destructive evaluation and non-contact food safety screening applications. This packaged ultra-wideband transceiver chipset offers a promising solution for low-cost field-deployable mm-wave/THz hyperspectral imaging.

REFERENCES

[1] C. Balanis, *Antenna Theory: Analysis and Design*, 3rd ed. New York, USA: J. Wiley & Sons, 2005.

[2] S. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Boston, MA, USA: Artech House, 2006.

[3] H. Wang, C. Sideris, and A. Hajimiri, "A CMOS broadband power amplifier with a transformer-based high-order output matching network," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2709–2722, Dec. 2010.

[4] H. Wang and K. Sengupta, *RF and Mm-Wave Power Generation in Silicon*. Cambridge, MA, USA: Academic Press, 2015.

[5] K. Russell, "Microwave power combining techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 27, no. 5, pp. 472–478, May 1979.

[6] E. Wilkinson, "An N-way hybrid power divider," *IEEE Trans. Microw. Theory Techn.*, vol. 8, no. 1, pp. 116–118, Jan. 1960.

[7] J. Taub and B. Fitzgerald, "A note on N-way hybrid power dividers," *IEEE Trans. Microw. Theory Techn.*, vol. 12, no. 2, pp. 260–261, Mar. 1964.

[8] F. Wang and H. Wang, "An N-way transformer based Wilkinson power divider in CMOS," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016.

[9] U. Gysel, "A new N-way power divider/combiner suitable for high-power applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 1975, pp. 116–118.

[10] I. Aoki, S. Kee, D. Rutledge, and A. Hajimiri, "Distributed active transformer–a new power-combining and impedance-transformation technique," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 1, pp. 316–331, Jan. 2002.

[11] I. Aoki, S. Kee, D. Rutledge and A. Hajimiri, "Fully integrated CMOS power amplifier design using the distributed active-transformer architecture," *IEEE J. Solid-State Circuits*, vol. 37, no. 7, pp. 371–383, Mar. 2002.

[12] Y. Wang, H. Wang, C. Hull, and S. Ravid, “A transformer-based broadband front-end combo in standard CMOS,” *IEEE J. Solid-State Circuits*, vol. 47, no. 8, pp. 1810–1819, Aug. 2012.

[13] P. Haldi, D. Chowdhury, P. Reynaert, G. Liu, and A. Niknejad, “A 5.8 GHz 1 V linear power amplifier using a novel on-chip transformer power combiner in standard 90 nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1054–1063, Apr. 2008.

[14] K. An *et al.*, “Power-combining transformer techniques for fully-integrated CMOS power amplifiers,” *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1064–1075, May 2008.

[15] T. Chi, J. Papapolymerou, and H. Wang, “A +2.3dBm 124-158GHz Class-C frequency quadrupler with folded-transformer based multi-phase driving,” in *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, May 2015, pp. 263–266.

[16] R. Bhar, A. Chakrabarti, and H. Krishnaswamy, “Large-scale power combining and mixed-signal linearizing architectures for watt-class mmWave CMOS power amplifiers,” *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 703–718, Feb. 2015.

[17] W. Tai, L. Carley, and D. Ricketts, “A 0.7W fully-integrated 42GHz power amplifier with 10% PAE in 0.13μm SiGe BiCMOS,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 142–143.

[18] K. Datta and H. Hashemi, “A 29dBm 18.5% peak PAE mm-wave digital power amplifier with dynamic load modulation,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 46–47.

[19] S. Pajić and Z. Popović, “An efficient X-band 16-element spatial combiner of switched-mode power amplifiers,” *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 7, pp. 1863–1870, July 2013.

[20] M. DeLisio and R. York, “Quasi-optical and spatial power combining,” *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 3, pp. 929–936, Mar. 2002.

[21] S. Joen *et al.*, “A scalable 6-to-18 GHz concurrent dual-band quad-beam phased array receiver in CMOS,” *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2660–2673, Dec. 2008.

[22] X. Guan, H. Hashemi, and A. Hajimiri, "A fully integrated 24-GHz eight-element phased-array receiver in silicon," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2311–2320, Dec. 2004.

[23] C. Patterson *et al.*, "A lightweight organic X-band active receiving phased array with integrated SiGe amplifiers and phase shifters," *IEEE Trans. Antennas Propag.*, vol. 59, no. 1, pp. 100–109, Jan. 2011.

[24] J. Park, T. Chi, and H. Wang, "An ultra-broadband compact mm-wave Butler Matrix in CMOS for array-based MIMO systems," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sept. 2013.

[25] S. Li *et al.*, "A fully packaged D-band MIMO transmitter using high-density flip-chip interconnects on LCP substrate," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016.

[26] G. Rebeiz, D. Kasilingam, Y. Guo, P. Stimson, and D. Rutledge, "Monolithic millimeter-wave two-dimensional horn imaging array," *IEEE Trans. Antennas Propag.*, vol. 38, no. 9, pp. 1473–1482, Sep. 1990.

[27] D. Shin and G. Rebeiz, "A high-linearity X-band four-element phased-array receiver: CMOS chip and packaging," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 8, pp. 2064–2072, Aug. 2011.

[28] S. Zihir, O. Gurbuz, A. Roy, S. Raman, and G. Rebeiz, "60-GHz 64- and 256-elements wafer-scale phased-array transmitters using full-reticle and subreticle stitching techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4701–4719, Dec. 2016.

[29] F. Golcuk, O. Gurbuz, and G. Rebeiz, "A 0.39–0.44 THz 2×4 amplifier-quadrupler array with peak EIRP of 3–4 dBm," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4483–4491, Dec. 2013.

[30] M. Huang, T. Chi, F. Wang, and H. Wang, "An all-passive negative feedback network for broadband and wide field-of-view self-steering beam-forming with zero DC power consumption" *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1260–1273, May 2017.

[31] M. Huang, T. Chi, and H. Wang, “A 5GHz all-passive negative feedback network for RF front-end self-steering beam-forming with zero DC power consumption,” in *Proc. IEEE RF Integrated Circuits Symp.*, May 2016, pp. 91–94.

[32] S. Li, T. Chi, J. Park, and H. Wang, “A multi-feed antenna for antenna-level power combining,” in *Proc. IEEE Int. Symp. Antennas Propag.*, June 2016.

[33] S. Li, T. Chi, Y. Wang, and H. Wang, “A millimeter-wave dual-feed square loop antenna for 5G communications,” accepted and to appear in *IEEE Trans. Antennas Propag.*

[34] S. Bowers and A. Hajimiri, “Multi-port driven radiators,” *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4428–4441, Dec. 2013.

[35] S. Bowers, A. Safaripour, and A. Hajimiri, “An integrated slot-ring traveling-wave radiator,” *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 4, pp. 1154–1162, Apr. 2015.

[36] S. Bowers, A. Safaripour, and A. Hajimiri, “Dynamic polarization control,” *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1224–1236, May 2015.

[37] P. Nazari, S. Jafarlou, and P. Heydari, “A fundamental-frequency 114GHz circular-polarized radiating element with 14dBm EIRP, −99.3dBc/Hz phase-noise at 1MHz offset and 3.7% peak efficiency,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 322–323.

[38] F. Cai, W. Khan, and J. Papapolymerou, “A low loss X-band filter using 3-D polyjet technology,” in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2015.

[39] T. Chi, *et al.*, “A 60GHz on-chip linear radiator with single-element 27.9dBm Psat and 33.1dBm peak EIRP using multifeed antenna for direct on-antenna power combining,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 296–297.

[40] T. Chi, H. Wang, M. Huang, F. Dai, and H. Wang, “A bidirectional lens-free digital-bits-in/-out 0.57mm^2 Terahertz nano-radio in CMOS with 49.3mW peak power consumption supporting 50cm Internet-of-Things communication,” in *Proc. IEEE Custom Integrated Circuits Conf.*, May 2017.

[41] B. Kormanyos, W. Harokopus, L. Katehi, and G. Rebeiz, "CPW-fed active slot antennas," *IEEE Trans. Microw. Theory Techn.*, vol. 42, no. 4, pp. 541–545, Apr. 1994.

[42] D. Pozar, *Microwave Engineering*, 4th ed. New York, USA: J. Wiley & Sons, 2011.

[43] R. King and T. Wu, "The cylindrical antenna with arbitrary driving point," *IEEE Trans. Antennas Propag.*, vol. 13, no. 5, pp. 710–718, Sep. 1965.

[44] R. Li, L. Pan, and Y. Cui, "A novel broadband circularly polarized antenna based on off-center-fed dipoles," *IEEE Trans. Antennas Propag.*, vol. 63, no. 12, pp. 5296–5304, Dec. 2015.

[45] R. Harrington, *Field Computation by Moment Methods*, New York, USA: Macmillan, 1968.

[46] W. Stutzman and G. Thiele, *Antenna Theory and Design*, 3rd ed. New York, USA: J. Wiley & Sons, 2012.

[47] M. Kashanianfard and K. Sarabandi, "An accurate circuit model for input impedance and radiation pattern of two-port loop antennas as E- and H-probe," *IEEE Trans. Antennas Propag.*, vol. 65, no. 1, pp. 114–120, Jan. 2017.

[48] N. Alexopoulos, P. Katehi, and D. Rutledge, "Substrate optimization for integrated circuit antenna," *IEEE Trans. Microw. Theory Techn.*, vol. 31, no. 7, pp. 550–557, July 1983.

[49] C. Balanis, "Pattern distortion due to edge diffractions," *IEEE Trans. Antennas Propag.*, vol. 18, no. 4, pp. 561–563, July 1970.

[50] J. Yun and R. Vaughan, "Open slot antenna in a small ground plane," *IET Microw. Antennas Propag.*, vol. 5, no. 2, pp. 200–213, Jan. 2011.

[51] T. Chi, J. Park, S. Li, and H. Wang, "A 64GHz full-duplex transceiver front-end with an on-chip multifeed self-interference-canceling antenna and an all-passive canceler supporting 4Gb/s modulation in one antenna footprint," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018.

[52] T. Dinc, *et al.*, "A 60GHz CMOS full-duplex transceiver and link with polarization-based antenna and RF cancellation," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1125-1140, May 2016.

[53] B. van Liempd, *et al.*, "A +70dBm IIP3 single-ended electrical balance duplexer in 0.18μm SOI CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 32-33.

[54] T. Dinc and H. Krishnaswamy, "A 28GHz magnetic-free non-reciprocal passive CMOS circulator based on spatio-temporal conductance modulation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 294-295.

[55] F.-W. Kuo *et al.*, "A Bluetooth Low-Energy transceiver with 3.7-mW all-digital transmitter, 2.75-mW high-IF discrete-time receiver, and TX/RX switchable on-chip matching network," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1144–1162, Apr. 2017.

[56] M. Babaie *et al.*, "A fully integrated Bluetooth Low-Energy transmitter in 28 nm CMOS with 36% system efficiency at 3 dBm," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1547–1564, July 2016.

[57] J. Prummel *et al.*, "A 10 mW Bluetooth Low-Energy transceiver with on-chip matching," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3077–3088, Dec. 2015.

[58] Y.-H. Liu *et al.*, "A 3.7mW-RX 4.4mW-TX fully integrated Bluetooth Low-Energy/IEEE802.15.4/proprietary SoC with an ADPLL-based fast frequency offset compensation in 40nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 236–237.

[59] X. Peng, J. Yin, P.-I. Mak, W.-H. Yu, and R. Martins, "A 2.4-GHz ZigBee transmitter using a function-reuse class-F DCO-PA and an ADPLL achieving 22.6% (14.5%) system efficiency at 6-dBm (0-dBm) P_{out}," *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1495–1508, June 2017.

[60] Z. Lin, P.-I. Mak, and R. Martins, "A sub-GHz multi-ISM-band ZigBee receiver using function-reuse and gain-boosted N-path techniques for IoT applications," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2990–3004, Dec. 2014.

[61] M. Tedeschi, A. Liscidini, and R. Castello, "Low-power quadrature receivers for ZigBee (IEEE 802.15.4) applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1710–1719, Sep. 2010.

[62] M. Rahman, M. Elbadry, and R. Harjani, "WBAN transmitter using phase multiplexing and injection locking," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1126–1136, May 2015.

[63] J. Cheng, N. Qi, P. Chiang, and A. Natarajan, "A low-power, low-voltage WBAN-compatible sub-sampling PSK receiver in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 3018–3030, Dec. 2014.

[64] A. Wong *et al.*, "A 1 V 5 mA multimode IEEE 802.15.6/Bluetooth Low-Energy WBAN transceiver for biotelemetry applications," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 186–198, Jan. 2013.

[65] Y. Shi *et al.*, "A 10mm^3 syringe-implantable near-field radio system on glass substrate," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 448–449.

[66] L.-X. Chuo *et al.*, "A 915MHz asymmetric radio using Q-enhanced amplifier for a fully integrated 3×3×3mm^3 wireless sensor node with 20m non-line-of-sight communication," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 132–133.

[67] K.-K. Huang *et al.*, "An ultra-low-power 9.8 GHz crystal-less UWB transceiver with digital baseband integrated 0.18 μm BiCMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3178–3189, Dec. 2013.

[68] B. Otis, Y. Chee, and J. Rabaey, "A 400μW-RX, 1.6mW-TX super-regenerative transceiver for wireless sensor networks," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2005, pp. 396–397.

[69] J. Im, H. Kim, and D. Wentzloff, " A 335μW -72dBm receiver for FSK back-channel embedded in 5.8GHz Wi-Fi OFDM packets," in *Proc. IEEE RF Integrated Circuits (RFIC) Symp.*, June 2017, pp. 176–179.

[70] S. Ikeda *et al.*, "A 0.5-V 5.8-GHz ultra-low-power RF transceiver for wireless sensor network in 65 nm CMOS," in *Proc. IEEE RF Integrated Circuits (RFIC) Symp.*, June 2014, pp. 29–32.

[71] M. Tabesh, N. Dolatsha, A. Arbabian, and A. Niknejad, “A power-harvesting pad-less millimeter-sized radio,” *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 962–977, Apr. 2015.

[72] J. Lien *et al.*, “Soli: ubiquitous gesture sensing with millimeter wave radar,” *ACM Trans. Graph.*, vol. 35, no. 4, pp. 1–19, July 2016.

[73] C. Li *et al.*, “A review on recent progress of portable short-range noncontact microwave radar systems,” *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 5, pp. 1692–1706, May 2017.

[74] M. Tonouchi, “Cutting-edge terahertz technology,” *Nature Photon.*, vol. 1, pp. 97–105, Feb. 2007.

[75] E. Carlson, K. Strunz, and B. Otis, “A 20 mV input boost converter with efficient digital control for thermoelectric energy harvesting,” *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 741–750, Mar. 2010.

[76] S. Pellerano, J. Alvarado, and Y. Palaskas, “A mm-wave power-harvesting RFID tag in 90 nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1627–1637, Aug. 2010.

[77] Y.-J. Wang, I.-N. Liao, C.-H. Tsai, and C. Pakasiri, “A millimeter-wave in-phase gate-boosting rectifier,” *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 11, pp. 2768–2783, Nov. 2014.

[78] H. Mamaghanian, N. Khaled, D. Atienza, and P. Vandergheynst, “Compressed sensing for real-time energy-efficient ECG compression on wireless body sensor nodes,” *IEEE Trans. Biomed. Eng.*, vol. 58, no. 9, pp. 2456–2466, Sep. 2011.

[79] F. Chen, A. Chandrakasan, and V. Stojanovic, “Design and analysis of a hardware-efficient compressed sensing architecture for data compression in wireless sensors,” *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 744–756, Mar. 2012.

[80] M. Shoaib, K. Lee, N. Jha, and N. Verma, “A 0.6–107 μW energy-scalable processor for directly analyzing compressive-sensed EEG,” *IEEE Trans. Circuits Syst. I*, vol. 61, no. 4, pp. 1105–1118, Jan. 2014.

[81] J. Park, S. Kang, and A. Niknejad, "A 0.38 THz fully integrated transceiver utilizing a quadrature push-push harmonic circuitry in SiGe BiCMOS," *IEEE Symp. VLSI Circuits*, pp. 22–23, June 2011.

[82] N. Sarmah, *et al.*, "A fully integrated 240-GHz direct-conversion quadrature transmitter and receiver chipset in SiGe technology," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 2, pp. 562–574, Feb. 2016.

[83] Z. Wang, P.-Y. Chiang, P. Nazari, C.-C. Wang, Z. Chen, and P. Heydari, "A CMOS 210-GHz fundamental transceiver with OOK modulation," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 564–580, Mar. 2014.

[84] R. Han *et al.*, "Active terahertz imaging using Schottky diodes in CMOS: array and 860-GHz pixel," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2296–2308, July 2013.

[85] T. Chi, M. Huang, S. Li, and H. Wang, "A packaged 90-to-300GHz transmitter and 115-to-325GHz coherent receiver in CMOS for full-band continuous-wave mm-wave hyperspectral imaging," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 304–305.

[86] A. Tang and M.-C. Chang, "183GHz 13.5mW/pixel CMOS regenerative receiver for mm-wave imaging applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 296–297.

[87] A. Tang and M.-C. Chang, "Inter-modulated regenerative CMOS receivers operating at 349 and 495 GHz for THz imaging applications," *IEEE Trans. THz Sci. Technol.*, vol. 3, no. 2, pp. 134–140, Dec. 2012.

[88] E. Armstrong, "Some recent developments of regenerative circuits," *Proc. IRE*, vol.10, no.4, pp. 244–260, Aug. 1922.

[89] D.Shi, N. Behdad, J.-Y. Chen, and M. Flynn, "A 5GHz fully integrated super-regenerative receiver with on-chip slot antenna in 0.13μm CMOS," *IEEE Symp. VLSI Circuits*, pp. 34–35, June 2008.

[90] J. Bohorquez, A. Chandrakasan, and J. Dawson, "Frequency-domain analysis of super-regenerative amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 2882–2894, Dec. 2009.

[91] F. Moncunill-Geniz, P. Palà-Schönwälder, and O. Mas-Casals, "A generic approach to the theory of superregenerative reception," *IEEE Trans. Circuits Syst. I*, vol. 52, no. 1, pp. 54–70, Jan. 2005.

[92] J. Bonet-Dalmau, F. Moncunill-Geniz, P. Palà-Schönwälder, F. Águila-López, and R. Giralt-Mas, "Frequency domain analysis of superregenerative receivers in the linear and logarithmic modes," *IEEE Trans. Circuits Syst. I*, vol. 59, no. 5, pp. 1074–1084, May 2012.

[93] H. Wang, F. Dai, and H. Wang, "A 330μW 1.25ps 400fs-INL vernier time-to-digital converter with 2D reconfigurable spiral arbiter array and 2nd-order ΔΣ linearization," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, May 2017.

[94] L. Vercesi, A. Liscidini and R. Castello, "Two-dimensions Vernier time-to-digital converter," *IEEE J. Solid-state Circuits*, vol. 45, no. 8, pp. 1504–1512, Aug. 2010.

[95] R. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg, and P. Balsara, "Time-to-digital converter for RF frequency synthesis in 90 nm CMOS," in *Proc. IEEE RF Integrated Circuits (RFIC) Symp.*, June 2005, pp. 473–476.

[96] J. Yu, F. Dai, and R. Jaeger, "A 12-bit vernier ring time-to-digital converter in 0.13 μm CMOS technology," *IEEE J. Solid-state Circuits*, vol. 45, no. 4, pp. 830–842, Apr. 2010.

[97] J. Yu and F. Dai, "A 3-dimensional vernier ring time-to-digital converter in 0.13μm CMOS," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, Sep. 2010.

[98] D. Liao, H. Wang, F. Dai, Y. Xu, R. Berenguer and S. Hermoso, "An 802.11a/b/g/n digital fractional-N PLL with automatic TDC linearity calibration for spur cancellation," *IEEE J. Solid-state Circuits*, vol. 52, no. 5, pp. 1210–1220, May 2017.

[99] N. Gopalsami, S. Bakhtiari, T. W. Elmer, and A. C. Raptis, "Application of millimeter-wave radiometry for remote chemical detection," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 3, pp. 700–709, Mar. 2008.

[100] P. H. Siegel, "Terahertz technology," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 3, pp. 910–928, Mar. 2002.

[101] K. B. Cooper, R. J. Dengler, N. Llombart, B. Thomas, G. Chattopadhyay, and P. H. Siegel, "THz imaging radar for standoff personnel screening," *IEEE Trans. Terahertz Sci. Technol.*, vol. 1, no. 1, pp.169–182, Sep. 2011.

[102] L. A. Samoska, "An overview of solid-state integrated circuit amplifiers in the submillimeter-wave and THz regime," *IEEE Trans. Terahertz Sci. Technol.*, vol. 1, no. 1, pp. 9–24, Sep. 2011.

[103] M. Tonouchi, "Cutting-edge terahertz technology," *Nature Photonics*, vol. 1, no. 2, pp. 97–105, Feb. 2007.

[104] R. Chamas and S. Raman, "Analysis and design of a CMOS phase tunable injection-coupled quadrature VCO (PTIC-QVCO)," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 784–796, Mar. 2009.

[105] P. Kinget, R. Melville, D. Long, and V. Gopinathan, "An injection-locking scheme for precision quadrature generation," *IEEE J. Solid-State Circuits*, vol. 37, no. 7, pp. 845–851, Jul. 2002.

[106] N. Lanka, S. Patnaik, and R. Harjani, "Frequency-hopped quadrature frequency synthesizer in 0.13-µm technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2021–2032, Sep. 2011.

[107] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.

[108] T. Chi, J. Luo, S. Hu, and H. Wang, "A multi-phase sub-harmonic injection locking technique for bandwidth extension in silicon-based THz signal generation", in *Proc. IEEE Custom Integrated Circuits Conf.,* 2014.

[109] T. Chi, J. Luo, S. Hu, and H. Wang, "A multi-phase sub-harmonic injection locking technique for bandwidth extension in silicon-based THz signal generation," *IEEE J. Solid-state Circuits,* vol. 50, no. 8, pp. 1861–1873, Aug. 2015.

[110] T. Chi and H. Wang, "A scalable active THz frequency multiplier chain in silicon with multi-phase sub-harmonic injection locking for bandwidth extension," in *Proc. IEEE Asia-Pacific Microwave Conf.,* Dec. 2015.

[111] Momeni and E. Afshari, "High power terahertz and millimeter-wave oscillator design: a systematic approach," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 583–597, Mar. 2011.

[112] U. R. Pfeiffer, *et al.*, "A 0.53THz reconfigurable source array with up to 1mW radiated power for terahertz imaging applications in 0.13µm SiGe BiCMOS," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2014, pp. 256–257.

[113] W. Steyaert and P. Reynaert, "A 0.54 THz signal generator in 40 nm bulk CMOS with 22 GHz tuning range and integrated planar antenna," *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp. 1617–1626, Jul. 2014.

[114] D. Shim, D. Koukis, D. Arenas, D. Tanner, and K. Kenneth, "553-GHz signal generation in CMOS using a quadruple-push oscillator," in *IEEE Symp. VLSI Circuits*, 2011, pp. 154–155.

[115] M. Adnan and E. Afshari, "A 247-to-263.5GHz VCO with 2.6mW peak output power and 1.14% DC-to-RF efficiency in 65nm bulk CMOS," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2014, pp. 262–263.

[116] R. Han and E. Afshari, "A CMOS high-power broadband 260-GHz radiator array for spectroscopy," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3090–3104, Dec. 2013.

[117] K. Sengupta and A. Hajimiri, "A 0.28 THz power-generation and beam-steering array in CMOS based on distributed active radiators," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3013–3031, Dec. 2012.

[118] J. Grzyb, Y. Zhao, and U. Pfeiffer, "A 288-GHz lens-integrated balanced triple-push source in a 65 nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1751–1761, Jul. 2013.

[119] Y. Tousi, O. Momeni, and E. Afshari, "A novel CMOS high-power terahertz VCO based on coupled oscillators: theory and implementation," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3032–3042, Dec. 2012.

[120] P.-Y. Chiang, Z. Wang, O. Momeni, and P. Heydari, "A 300 GHz frequency synthesizer with 7.9% locking range in 90 nm SiGe BiCMOS," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2014, pp. 260–261.

[121] J. Sharma and H. Krishnaswamy, "216- and 316-GHz 45-nm SOI CMOS signal sources based on a maximum-gain ring oscillator topology," *IEEE Trans. Microw. Theory Tech.,* vol. 61, no. 1, pp. 492–504, Jan. 2013.

[122] S. P. Voinigescu, A. Tomkins, E. Dacquay, P. Chevalier, J. Hasch, A. Chantre, and B. Sautreuil, "A Study of SiGe HBT signal sources in the 220–330-GHz range," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2011–2021, Sep. 2013.

[123] Y. Tousi and E. Afshari, "A scalable THz 2D phased array with +17 dBm of EIRP at 338 GHz in 65 nm bulk CMOS," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.,* 2014, pp. 258–259.

[124] E. O. Johnson, "Physical limitations on frequency and power parameters of transistors," *RCA Rev.*, vol. 26, pp. 163–177, 1965.

[125] K. Cooper, *et al.*, "Penetrating 3-D imaging at 4- and 25-m range using a submillimeter-wave radar" *IEEE Trans. Microw. Theory Tech.,* vol. 56, no. 12, pp. 2771–2778, Dec. 2008.

[126] A. Mirzaei, M. E. Heidari, R. Bagheri, and A. A. Abidi, "Multi-phase injection widens lock range of ring-oscillator-based frequency dividers," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 656–671, Mar. 2008.

[127] A. Mirzaei, M. E. Heidari, R. Bagheri, S. Chehrazi, and A. A. Abidi, "The quadrature LC oscillator: A complete portrait based on injection locking," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1916–1932, Sep. 2007.

[128] T. Chi, J. S. Park, R. L. Schmid, A. C. Ulusoy, J. D. Cressler, and H. Wang, "A low-power and ultra-compact W-band transmitter front-end in 90 nm SiGe BiCMOS Technology," in *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 2014.

[129] J. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.

[130] W. Khan, A. Lopez, A. Ulusoy, and J. Papapolymerou, "Packaging a W-band integrated module with an optimized flip-chip interconnect on an organic substrate", *IEEE Trans. Microw. Theory Tech.,* vol. 62, no. 1, pp. 64-72, Jan. 2014.

[131] Y. Li, I. Mehdi, A. Maestrini, R. Lin, and J. Papapolymerou, "A broadband 900-GHz silicon micromachined two-anode frequency tripler," *IEEE Trans. Microw. Theory Tech.,* vol. 59, no. 6, pp. 1673-1681, Jun. 2011.

[132] P. Kirby, D. Pukala, H. Manohara, I. Mehdi and J. Papapolymerou, "Characterization of micromachined silicon rectangular waveguide at 400 GHz," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 6, pp. 366-368, Jun. 2006.

[133] Dominion MicroProbes Inc. Charlottesville, VA 22905, USA. [Online] Available: http://www.dmprobes.com/ProductsDMPI.html

[134] Virginia Diodes, Inc. Charlottesville, VA 22902, USA. [Online] Available: http://vadiodes.com/index.php/en/

[135] C.-I. Chang, *Hyperspectral Imaging: Techniques for Spectral Detection and Classification*, Springer Science & Business Media, 2003.

[136] H. Grahn, Paul Geladi, *Techniques and Applications of Hyperspectral Image Analysis*, John Wiley & Sons, 2007.

[137] K. Statnikov, et al., "160-GHz to 1-THz multi-color active imaging with a lens-coupled SiGe HBT chip-set", *IEEE Trans. Microw. Theory Techn.,* vol. 63, no. 2, pp. 520–532, Feb. 2015.

[138] C. Jiang, et al., "A 320GHz subharmonic-mixing coherent imager in 0.13μm SiGe BiCMOS," *ISSCC Dig. Tech. Papers*, pp. 432–433, Feb. 2016.

[139] N. Sharma, et al., "160-310 GHz frequency doubler in 65-nm CMOS with 3-dBm peak output power for rotational spectroscopy", *IEEE Radio Frequency Integrated Circuits Symp.,* pp. 186–189, May 2016.

[140] Q. Zhong, et al., "A 210-to-305GHz CMOS receiver for rotational spectroscopy", *ISSCC Dig. Tech. Papers*, pp. 426–427, Feb. 2016.

[141] J. Chen and A. Niknejad, "Design and analysis of a stage-scaled distributed power amplifier", *IEEE Trans. Microw. Theory Techn.,* vol. 59, no. 5, pp. 1274–1283, May 2011.